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Lifetime Extension Method for Three-Phase Voltage Source Converters Using Discontinuous PWM Scheme with Hybrid Offset Voltage

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Abstract: This paper proposes a lifespan extension technique for three-phase voltage inverters using hybrid offset voltage. The proposed method lengthens the inverter lifetime by independently adjusting the switching frequency of the three phases in accordance with the aging degree. To reduce the switching operation of the phase with the shortest lifetime, the proposed technique injects the offset voltage for generalized discontinuous pulse-width modulation PWM (GDPWM) into the reference voltage in the region where the switching operation of the shortest lifespan phase can be stopped. When the switching operation does not need to be stopped, the offset voltage for space vector PWM (SVPWM) is injected into the reference voltage for high inverter load current quality. An offset voltage that varies according to the need to stop the switching operation is the proposed hybrid offset voltage. Using the proposed hybrid offset voltage, the switching frequencies of the three phases are independently controllable. In addition, since only the switching operation of the phase having the shortest lifespan is reduced, the load current quality in accordance with the switching operation reduction is good compared to the conventional method to simultaneously diminish all phase switching frequencies. The proposed method significantly increases the reliability of the three-phase voltage inverter, where the thermal stress of the phase having the shortest lifespan is decreased up to 55%, whereas the inverter lifetime can be increased by 10 times. The proposed technique was verified by simulations and experiments.

Keywords: lifetime extension; SiC MOSFET; gate oxide degradation; switching frequency; space vector PWM; discontinuous PWM; three-phase voltage source inverter; junction temperature



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1. Introduction

As a solution to rapid climate change caused by the use of fossil fuels, the dissemination of electric vehicles is increasing. Accordingly, the reliability of a three-phase inverter driving a motor of an electric vehicle is also becoming important. In particular, three-phase inverters based on SiC MOSFETs are used for high-efficiency electric vehicles [1]. SiC MOSFETs are attracting attention as highly efficient switching devices because of their small switching and conduction losses [2]. A lot of research has been conducted on the reliability of SiC MOSFETs. Typical types of degradation that SiC MOSFETs experience are chip-level degradation and package-level degradation [3]. When chip-level and package-level degradations occur, threshold voltage and on-resistance of SiC MOSFETs change [1,4].

Meanwhile, the overall converter lifetime is determined by the shortest lifespan component among the various converter components. The switching device is regarded as the shortest lifespan element among the converter components [5]. The junction temperature greatly influences the switching element lifespan [6]. Since losses raise the junction temperature, research has been conducted to extend converter life by reducing converter losses [7–12]. The method of reducing the loss of the converter to extend the lifespan is divided into a variable switching frequency method (VSFM) [7–9] and a method based on

discontinuous PWM (DPWM) [10–13]. In the VSFM, the number of switching operations varies to reduce the converter loss. In addition, in the DPWM-based method, the total converter loss is diminished by reducing the switching loss through the clamping angle adjustment. In addition to the converter life extension method through converter loss reduction, a method using reactive power [14] and a method using switch redundancy [15] have also been proposed. One of the significant advantages of model predictive control (MPC) is its flexibility to control multiple objectives simultaneously. In the MPC methods considering the increase in converter lifetime, an additional cost function is added to reduce the number of switching transitions, along with other control objectives [16,17].

As mentioned earlier, various studies have been conducted on the aging characteristics of SiC MOSFETs, but few studies have researched the effect of aging SiC MOSFETs on the converter lifespan. In addition, a lot of methods for extending the converter lifetime have been developed, but no research has dealt with extending the lifespan reduced by aging SiC MOSFETs. Additionally, limited research considers the different aging conditions in three-phase voltage inverters. This paper proposes a technique to lengthen the lifespan of a three-phase voltage source inverter (VSI) composed of aged SiC MOSFETs using hybrid offset voltage. Moreover, a three-phase VSI lifetime prediction simulator based on the electrical characteristics of SiC MOSFET is proposed. Through the developed inverter lifetime prediction simulator, the effect of aged SiC MOSFET on the three-phase VSI lifespan was analyzed and the lifetime extension effect of the proposed technique was confirmed. The proposed method significantly increases the reliability of the three-phase voltage inverter, where the thermal stress of the phase having the shortest lifespan is decreased and the lifetime of the entire VSI is prolonged.

The structure of this paper after the introduction is as follows. Section 2 is a description of conventional carrier-based PWM. Section 3 explains the proposed lifetime extension method using hybrid offset voltage. Sections 4 and 5 verify the proposed method using the simulations and experiments. Section 6 presents an analysis of the lifetime extension effect of the proposed technique. Section 7 compares the load current quality and losses of the proposed and conventional methods. Section 8 is the conclusion of this paper.

2. Carrier-Based PWM

A three-phase VSI is used for various purposes, such as driving a motor or connecting to a grid. Figure 1 shows a three-phase VSI composed of SiC MOSFETs. In Figure 1, V_{dc} and C_{dc} represent the inverter input voltage and DC-link capacitor, respectively. In addition, S_1 to S_6 mean SiC MOSFETs, which are switching devices. The three-phase motor, which is the inverter load, is expressed by the load inductor (L), the load resistor (R) and the back electromotive force (EMF). i_{La} denotes the a -phase load current.

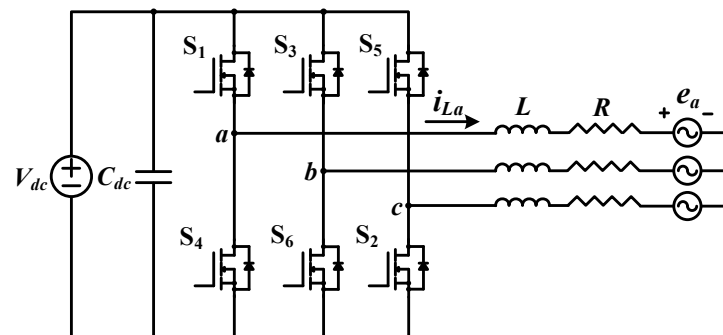


Figure 1. Circuit diagram of three-phase VSI.

A conventional method to create a switching signal that controls a three-phase VSI, as shown in Figure 1, is to compare the carrier with a reference voltage. This method is called carrier-based PWM. Carrier-based PWM can achieve various control purposes by injecting different offset voltages into the reference voltage of each phase.

Figure 2 depicts how switching signals are generated in the carrier-based PWM. In Figure 2, v_{rx} means the reference voltages of the x -phase ($x = a, b, c$). In addition, v_{off} represents the offset voltage. Figure 2 demonstrates that the switching signals of the three-phase VSI are generated by comparing the carrier with the reference voltage plus the offset voltage. Equation (1) represents v_{rx_off} ($x = a, b, c$), the x -phase reference voltage plus the offset voltage. Depending on which voltage is used as the offset voltage in Equation (1), the control technique of the inverter is different.

$$\begin{aligned} v_{ra_off} &= v_{ra} + v_{off}, \\ v_{rb_off} &= v_{rb} + v_{off}, \\ v_{rc_off} &= v_{rc} + v_{off}. \end{aligned} \quad (1)$$

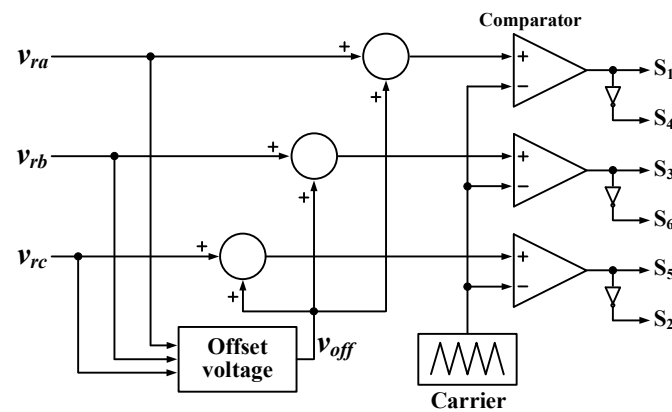


Figure 2. Carrier-based PWM.

2.1. Space Vector PWM

Space vector PWM (SVPWM) is a method to control three-phase VSIs because of its excellent load current quality and high maximum modulation. SVPWM is implemented by applying the following voltage as an offset voltage Equation (2) [18].

$$v_{off_sv} = -0.5(v_{rmax} + v_{rmin}). \quad (2)$$

In Equation (2), v_{off_sv} means the offset voltage for SVPWM. In addition, v_{rmax} and v_{rmin} denote the maximum and minimum among v_{ra} , v_{rb} and v_{rc} , respectively. Figure 3 shows v_{ra} , v_{off_sv} and v_{ra_sv} , which is the sum of v_{ra} and v_{off_sv} when SVPWM is applied.

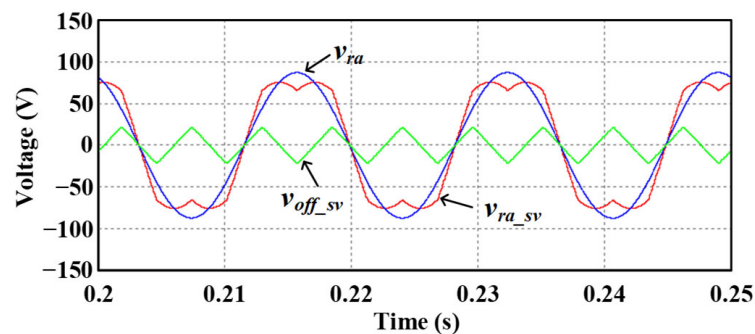


Figure 3. v_{ra} , v_{off_sv} , and v_{ra_sv} when SVPWM is applied.

2.2. Generalized Discontinuous PWM

DPWM is characterized in that switching loss can be reduced because the switching operation is stopped in a specific period. When a three-phase VSI is controlled by DPWM, the switching operation is stopped by 120° per phase. Among various DPWM techniques, the generalized DPWM (GDPWM) can effectively decrease the inverter switching loss

because the switching operation is stopped when the absolute load current is the largest. GDPWM is implemented by applying an offset voltage calculated by Equation (3) [19].

$$v_{off_d} = \begin{cases} 0.5V_{dc} - v_{rmax}, & \text{if } |i_{max}| > |i_{min}| \\ -0.5V_{dc} - v_{rmin}, & \text{if } |i_{min}| > |i_{max}| \end{cases} \quad (3)$$

In Equation (3), v_{off_d} means the offset voltage to implement GDPWM. In addition, i_{max} represents the load current in the phase with the largest reference voltage. Conversely, i_{min} is the load current in the phase with the smallest reference voltage. Figure 4 shows i_{La} , v_{ra} , v_{off_d} and v_{ra_d} , the sum of v_{ra} and v_{off_d} when GDPWM is applied. The switching operation can be stopped by setting v_{ra_d} to $V_{dc}/2$ or $-V_{dc}/2$ when the absolute load current is the largest using v_{off_d} . This operation can reduce switching loss.

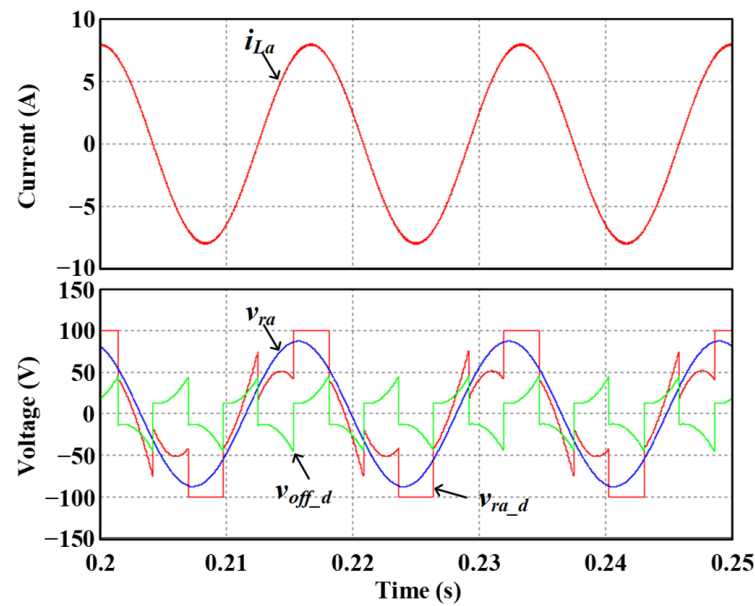


Figure 4. i_{La} , v_{ra} , v_{off_d} , and v_{ra_d} when GDPWM is applied.

The proposed method independently regulates the switching frequencies of all phases in the three-phase VSI using the hybrid offset voltage, a mixture offset voltage of SVPWM and GDPWM. This hybrid offset voltage effectively extends the inverter lifespan while mitigating load current quality deterioration.

3. Proposed Inverter Lifetime Extension Method Using Hybrid Offset Voltage

The three-phase inverter consists of 6 switching devices, as shown in Figure 1. Switching devices show different aging degrees under the same aging conditions [1,4]. Therefore, switching devices constituting one inverter have different aging rates under the same operating conditions. Since the inverter lifespan is decided by the most aged switching device, in this paper, the inverter lifespan is extended by regulating only the switching operation of the phase with the shortest lifetime.

Several techniques for monitoring the aging of switches have been proposed [20–22]. In [20], the on-resistance of the switching device was used for the aging monitoring. In addition, turn-on time or drain-source voltage was used to estimate the switching device aging [21,22]. Since the aging monitoring method of the switching device is out of the scope of this paper, a detailed description is not covered.

3.1. Hybrid Offset Voltage

The region where the switching operation is stopped in the DPWM is called the clamping region. There are studies that regulate the switching frequencies of all phases by changing the width of the clamping region of DPWM and that extend the converter

lifespan [10–12]. In these studies, the width of all phase clamping regions of the converter was varied equally. However, these methods regulate the switching frequencies of all phases equally without considering the aging of each phase, further deteriorating the load current quality. Since the overall converter lifetime is determined by the shortest lifespan phase, reducing only the switching frequency of the most aged phase can extend the overall converter lifetime. Therefore, the proposed scheme only stops the switching operation of the phase having the shortest lifetime in the clamping region, thereby increasing the overall lifespan of the converter and mitigating the degradation of the converter output quality.

In the proposed technique, individual phase switching frequency control is achieved using the hybrid offset voltage, the mixed offset voltage of SVPWM and GDPWM expressed in Equations (2) and (3). In the phase where the switching frequency needs to be reduced, v_{off_d} is used in the clamping region suitable for that phase and v_{off_sv} is used in the remaining region, called the non-clamping region, to obtain high-quality load current. The load current quality of SVPWM is better than sinusoidal PWM (SPWM), which controls the inverter with zero offset voltage [23]. Therefore, the inverter is controlled by SVPWM in the non-clamping region. Equation (4) represents the proposed hybrid offset voltage. In Equation (4), v_{off_hy} means the proposed hybrid offset voltage.

$$v_{off_hy} = \begin{cases} v_{off_sv}, & \text{in non-clamping region} \\ v_{off_d}, & \text{in clamping region} \end{cases} \quad (4)$$

Figure 5 shows the results when a three-phase inverter is controlled by the proposed hybrid offset voltage. In Figure 5, assuming that the most aged phase is a -phase, clamping operation is performed during the one-third period of a -phase. Figure 5 indicates that v_{off_d} is injected into the reference voltage to stop the a -phase switching operation when the largest load current flows in the a -phase. In addition, v_{off_sv} is injected in the remaining region.

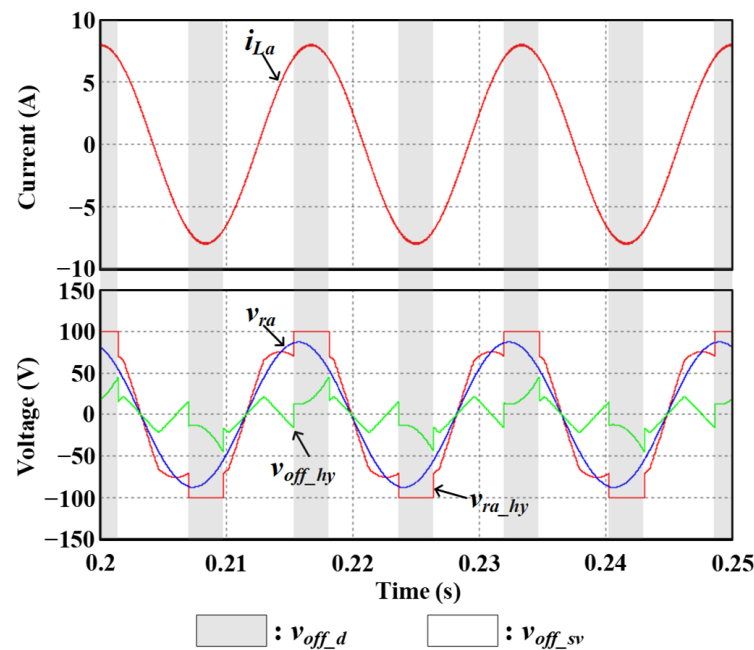


Figure 5. i_{La} , v_{ra} , v_{off_sv} , and v_{ra_hy} when the proposed hybrid offset voltage is applied.

$$\begin{aligned} v_{ra_hy} &= v_{ra} + v_{off_hy}, \\ v_{rb_hy} &= v_{rb} + v_{off_hy}, \\ v_{rc_hy} &= v_{rc} + v_{off_hy} \end{aligned} \quad (5)$$

Equation (5) represents the reference voltages plus the hybrid offset voltage. These reference voltages are compared with the carriers to generate a switching signal for the

inverter control. In Equation (5), v_{rx_hy} is the reference voltage of x -phase ($x = a, b, c$) plus the hybrid offset voltage.

3.2. Determination of Clamping Region

The switching operation is stopped in the specific region by the proposed technique. The load currents determine the region to stop the switching operation.

Figure 6 shows how to determine the clamping region of a -phase. In Figure 6, θ_a means the clamping angle of a -phase. The clamping angle determines the width of the clamping region. The range of θ_a is 0° to 60° . This is because the switching operation can be halted for one-third of the period per phase. In Figure 6, UC_{au} , UC_{al} , LC_{au} and LC_{al} are the upper limit for upper clamping in a -phase, the lower limit for upper clamping in a -phase, the upper limit for lower clamping in a -phase and the lower limit for lower clamping in a -phase, respectively.

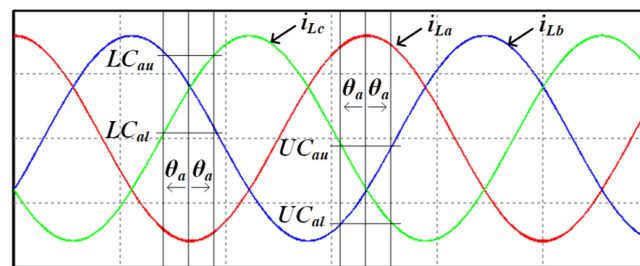


Figure 6. Determination of clamping region in a -phase.

Figure 6 shows that the a -phase upper clamping region is when i_{Lb} and i_{Lc} are between UC_{au} and UC_{al} . Moreover, the a -phase lower clamping region is when i_{Lb} and i_{Lc} are between LC_{au} and LC_{al} . In other words, the clamping region can be determined using the two-phase load currents.

Equation (6) shows how to calculate UC_{xu} , UC_{xl} , LC_{xu} and LC_{xl} ($x = a, b, c$). In Equation (6), i_{Lpeak} means the peak load current. Furthermore, θ_b and θ_c denote the clamping angle of the b -phase and c -phase, respectively.

$$\begin{aligned} UC_{xu} &= i_{Lpeak} \cos(120^\circ - 0.5\theta_x), \\ UC_{xl} &= i_{Lpeak} \cos(120^\circ + 0.5\theta_x), \\ LC_{xu} &= i_{Lpeak} \cos(60^\circ - 0.5\theta_x), \\ LC_{xl} &= i_{Lpeak} \cos(60^\circ + 0.5\theta_x). \end{aligned} \quad (6)$$

$(0^\circ \leq \theta_x \leq 60^\circ, x = a, b, c)$

Moreover, Table 1 summarizes the conditions for determining the clamping regions of all phases.

Table 1. Condition for clamping region determination.

Phase	Clamping Region	Condition
a -phase	Upper	$UC_{al} < i_{Lb} < UC_{au}$ and $UC_{al} < i_{Lc} < UC_{au}$
	Lower	$LC_{al} < i_{Lb} < LC_{au}$ and $LC_{al} < i_{Lc} < LC_{au}$
b -phase	Upper	$UC_{bl} < i_{Lc} < UC_{bu}$ and $UC_{bl} < i_{La} < UC_{bu}$
	Lower	$LC_{bl} < i_{Lc} < LC_{bu}$ and $LC_{bl} < i_{La} < LC_{bu}$
c -phase	Upper	$UC_{cl} < i_{La} < UC_{cu}$ and $UC_{cl} < i_{Lb} < UC_{cu}$
	Lower	$LC_{cl} < i_{La} < LC_{cu}$ and $LC_{cl} < i_{Lb} < LC_{cu}$

Figure 7 is a flow chart showing the method of determining the proposed hybrid offset voltage. Figure 7 demonstrates that the proposed hybrid offset voltage is calculated through the two-phase load current, UC_{xu} , UC_{xl} , LC_{xu} and LC_{xl} ($x = a, b, c$).

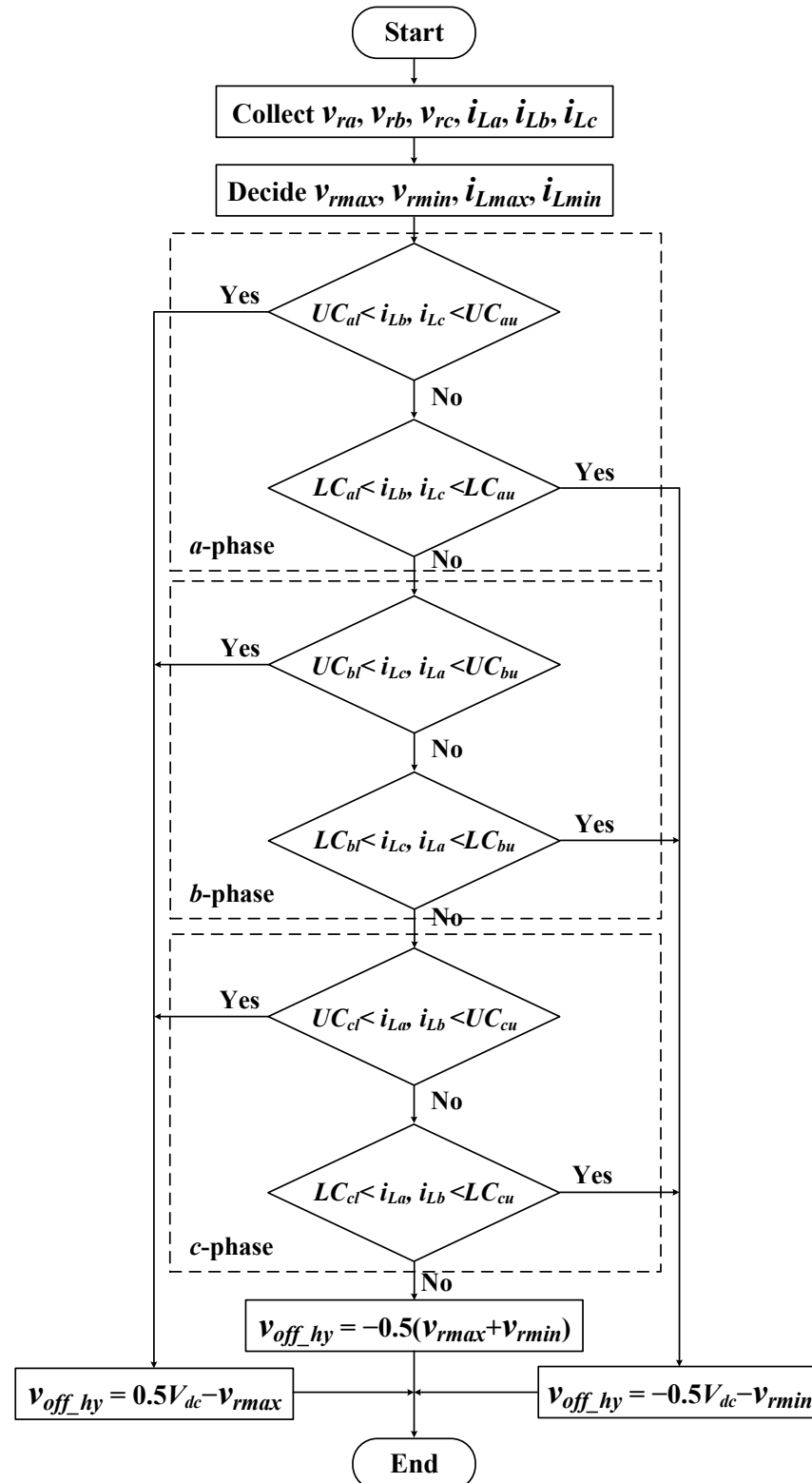


Figure 7. Flow chart for determination of proposed hybrid offset voltage.

Figure 8 represents the control block of the inverter lifetime extension method based on the proposed hybrid offset voltage. In Figure 8, i_{rLd} and i_{rLq} mean the references of the d - and q -axis load currents, respectively. Moreover, i_{Ld} and i_{Lq} indicate the d - and q -axis load currents, respectively. θ_{ri} is the reference angle of the load current. By regulating the clamping angles of the three phases, the proposed method can control the switching frequencies of the three phases. By preferentially reducing the switching frequency of the phase with the shortest lifespan, it is possible to effectively lengthen the inverter lifespan and mitigate the deterioration of the inverter load current quality caused by the switching frequency reduction. Furthermore, the lifespan of the inverter can be further extended by appropriately adjusting all phase switching frequencies, not just the most aged phase.

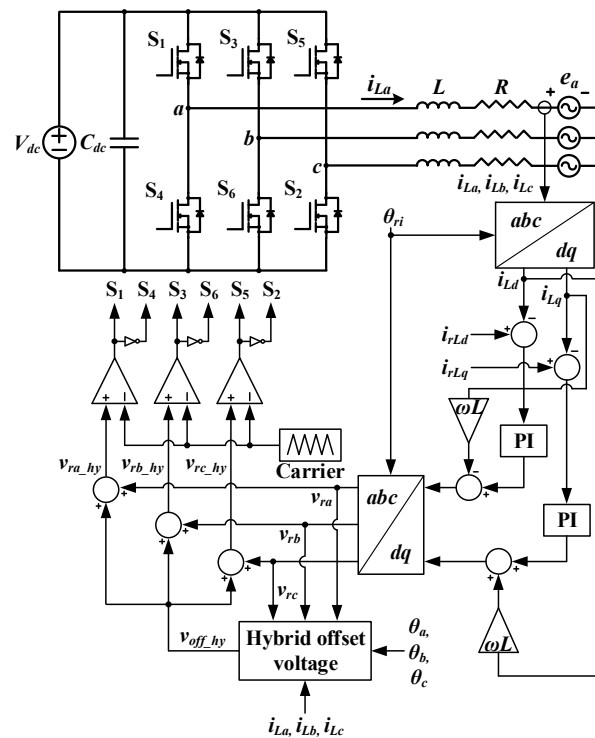


Figure 8. Control block of proposed inverter lifetime extension method using hybrid offset voltage.

4. Simulation Results

This section verifies the proposed method through the simulation. Table 2 summarizes the simulation parameters. A three-phase R-L load was used as the inverter load in the simulation.

Table 2. Simulation parameters used in this paper.

Parameters	Value
L	10 mH
R	10 Ω
C_{dc}	680 μ F
V_{dc}	200 V
i_{Lpeak}	8 A
Frequency of reference load current	60 Hz
Carrier frequency	20 kHz

The simulation results obtained from the proposed inverter lifetime extension method using hybrid offset voltage according to clamping angles are depicted in Figure 9. Figure 9

represents i_{La} , i_{Lb} , i_{Lc} and switching signals of S_1 , S_3 and S_5 . Figure 9a is in $\theta_a = \theta_b = \theta_c = 0^\circ$. Furthermore, Figure 9b is in $\theta_a = 30^\circ$ and $\theta_b = \theta_c = 0^\circ$. Moreover, Figure 9c is in $\theta_a = 60^\circ$ and $\theta_b = \theta_c = 0^\circ$. Figure 9a–c indicates that the a -phase switching operation can be stopped without halting the b - and c -phase switching operations. In addition, as θ_a increases, the region where the a -phase switching operation stops increases. Meanwhile, Figure 9d represents the simulation results when θ_a , θ_b and θ_c are set to 60° , 15° and 45° , respectively. Figure 9d demonstrates that the clamping regions of each phase can be controlled by setting the clamping angle of each phase differently.

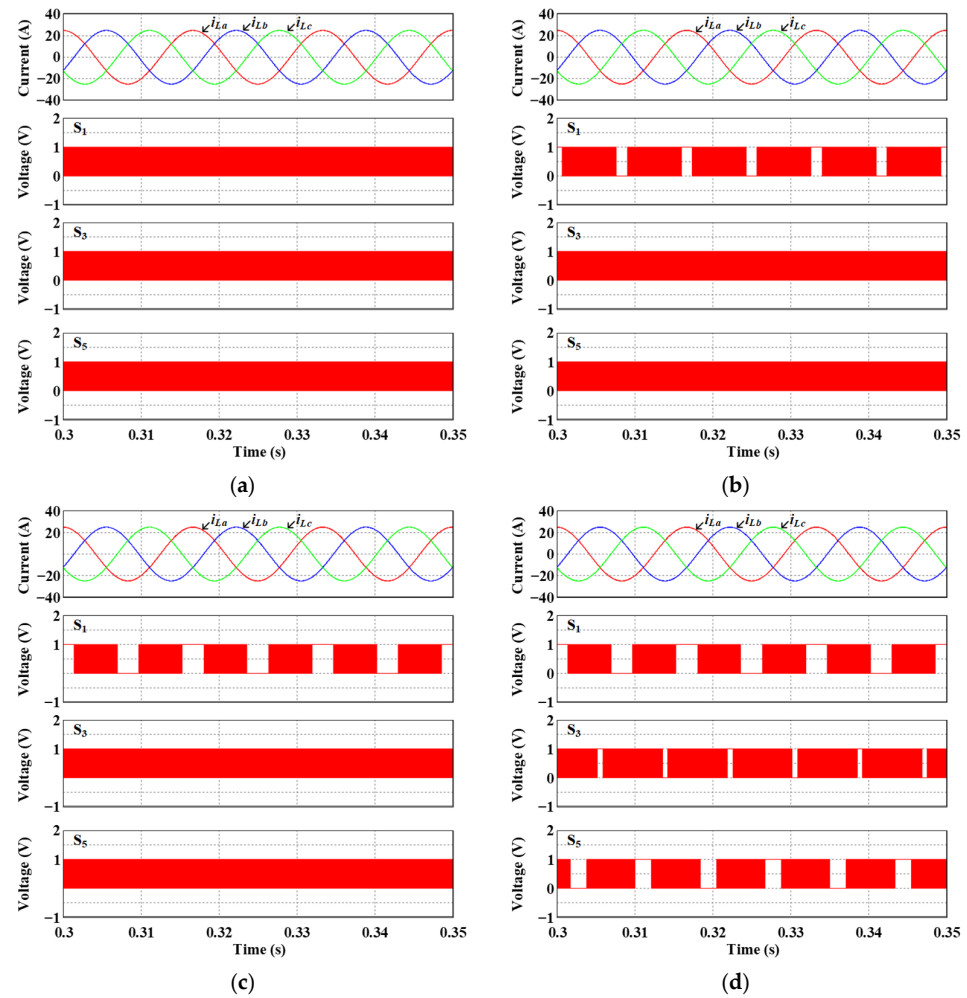


Figure 9. Simulation results of i_{La} , i_{Lb} , i_{Lc} , and switching signals of S_1 , S_3 , and S_5 obtained from the proposed method according to clamping angles (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (b) $\theta_a = 30^\circ$, $\theta_b = \theta_c = 0^\circ$ (c) $\theta_a = 60^\circ$, $\theta_b = \theta_c = 0^\circ$ (d) $\theta_a = 60^\circ$, $\theta_b = 15^\circ$, $\theta_c = 45^\circ$.

The simulation results of the three-phase load current, three-phase reference voltage plus offset voltage and offset voltage obtained from the proposed method according to clamping angles are represented in Figure 10. Figure 10a is the result when the three-phase clamping angles are 0° . Since the three-phase clamping angles are 0° , it operates as SVPWM in all regions. On the other hand, Figure 10b is the result in the case of $\theta_a = 30^\circ$ and $\theta_b = \theta_c = 0^\circ$. Additionally, Figure 10c is obtained under the condition of $\theta_a = 60^\circ$ and $\theta_b = \theta_c = 0^\circ$. Figure 10b,c demonstrates that as θ_a increases, the range operating as GDPWM increases. Figure 10d is when all three phase clamping angles are set differently. Figure 10d demonstrates that the region operating as GDPWM changes according to the clamping angle of each phase.

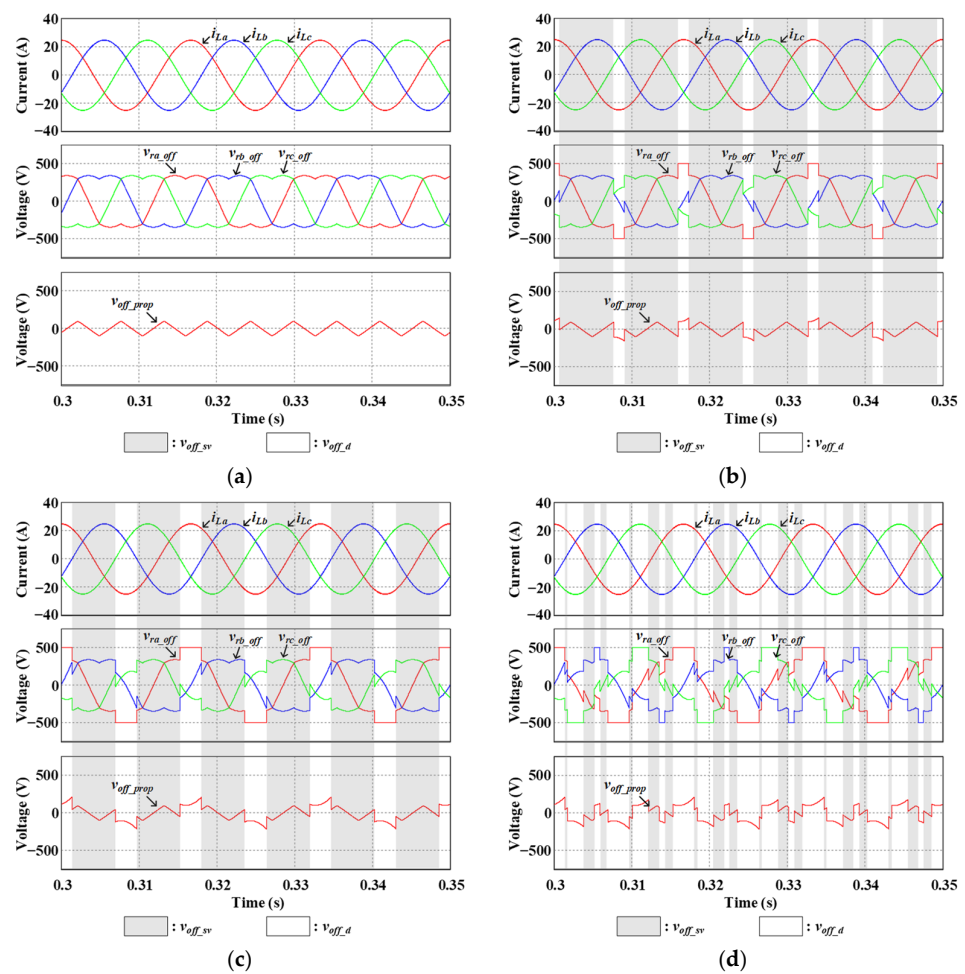


Figure 10. Simulation results of the three-phase load current, three-phase reference voltage plus offset voltage, and offset voltage obtained from the proposed method according to clamping angles (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (b) $\theta_a = 30^\circ, \theta_b = \theta_c = 0^\circ$ (c) $\theta_a = 60^\circ, \theta_b = \theta_c = 0^\circ$ (d) $\theta_a = 60^\circ, \theta_b = 15^\circ, \theta_c = 45^\circ$.

Figure 11 shows the switching frequencies of three phases when θ_a changes while θ_b and θ_c are maintained at 0° . The results in Figure 11 were obtained from the simulation. Figure 11 indicates that the b - and c -phase switching frequencies do not change and only the a -phase switching frequency can be controlled independently. In addition, the desired switching frequency can be obtained by regulating the clamping angle.

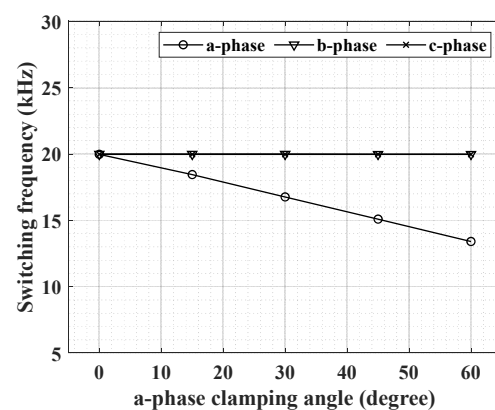


Figure 11. Switching frequencies of three phases according to a -phase clamping angle variation in $\theta_b = \theta_c = 0^\circ$ (obtained from simulation).

5. Experimental Results

This section confirms the performance of the proposed inverter lifespan extension technique through experiments. The parameters used in the experiment are the same values in Table 2. In addition, the three-phase R-L load was used as the inverter load in the experiment. Moreover, the digital signal processor used to control the three-phase VSI is TMS320F28335 (Texas Instruments, Dallas, TX, USA). The three-phase inverter consists of SiC MOSFETs (SCT3080AL, Rohm Semiconductor, Kyoto, Japan). The gate driver used is the SKHI22BR. Figure 12 represents the experimental setup used in this paper.

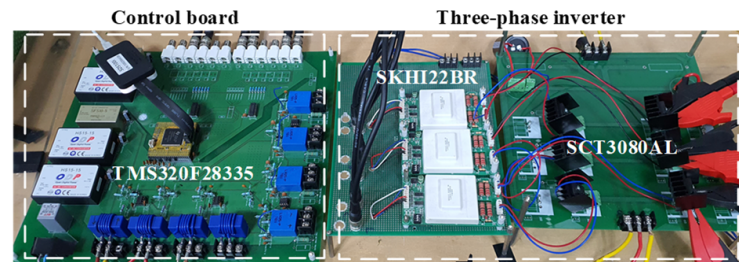


Figure 12. Experimental setup.

The experimental results of i_{La} and switching signals of S_1 , S_3 and S_5 obtained from the proposed method according to clamping angles are represented in Figure 13. Figure 13 implies that the proposed technique can independently control the three-phase clamping regions. In Figure 13a, all three phase clamping angles are set to 0° , in which the inverter is operated as the SVPWM. In Figure 13b, all three phase clamping angles are set to 60° , in which the inverter is operated as the GDPWM. Figure 13a,c,d represents that the proposed method can control the a -phase clamping region while the b - and c -phases are in the continuous switching operation. Moreover, Figure 13e demonstrates that the proposed technique can regulate the width of the three-phase clamping regions differently.

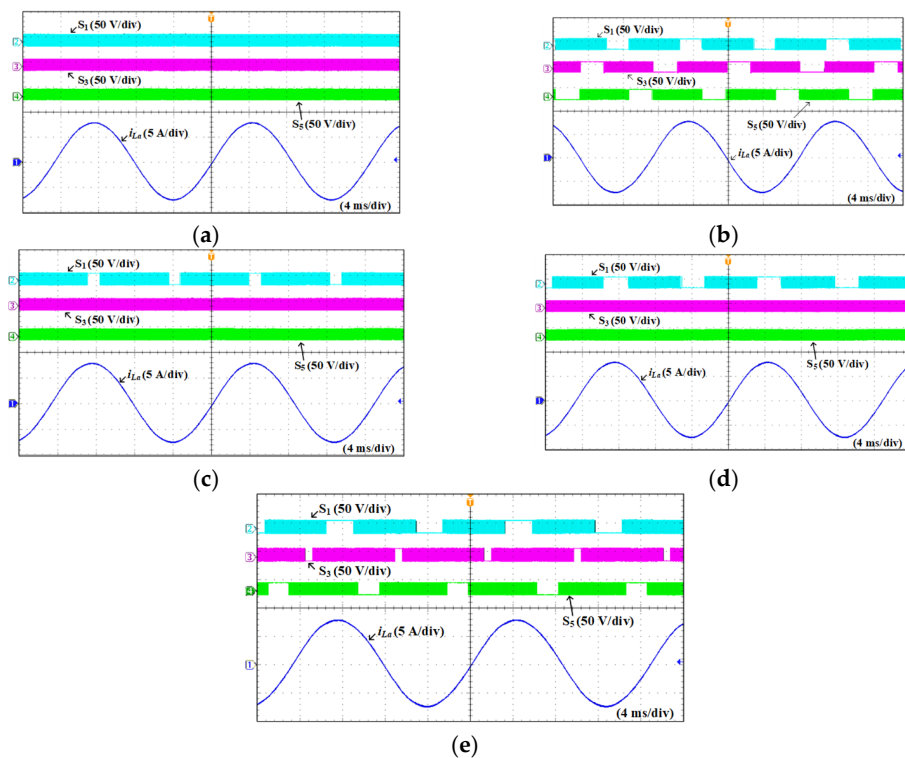


Figure 13. Experimental results of i_{La} and switching signals of S_1 , S_3 and S_5 obtained from the proposed method according to clamping angles (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (SVPWM) (b) $\theta_a = \theta_b = \theta_c = 60^\circ$ (GDPWM) (c) $\theta_a = 30^\circ$, $\theta_b = \theta_c = 0^\circ$ (d) $\theta_a = 60^\circ$, $\theta_b = \theta_c = 0^\circ$ (e) $\theta_a = 60^\circ$, $\theta_b = 15^\circ$, $\theta_c = 45^\circ$.

Figure 14 shows the experimental results of i_{La} , i_{Lb} , i_{Lc} and the switching signal of S_1 obtained from the proposed method according to clamping angles. Figure 14 represents that the three-phase load current is well controlled as a sinusoidal waveform under the reduction in the a -phase switching operation.

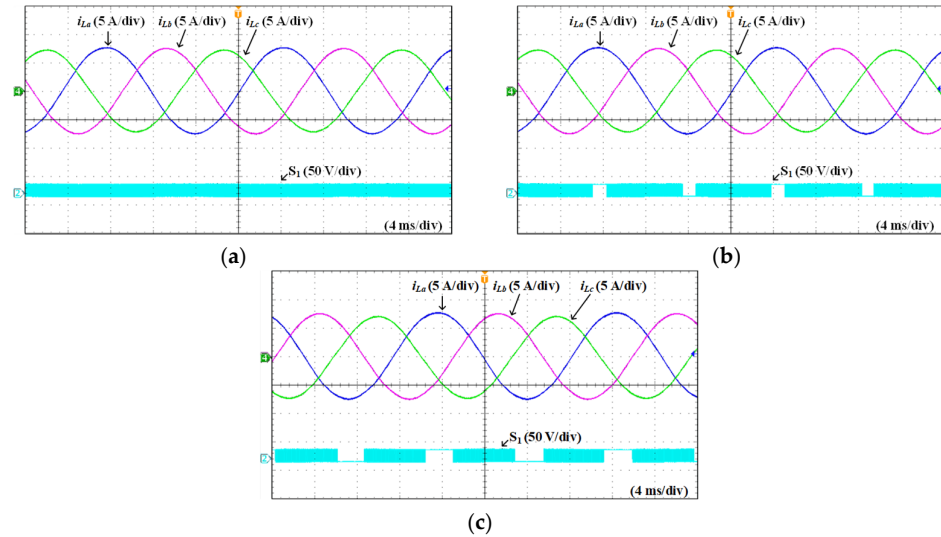


Figure 14. Experimental results of i_{La} , i_{Lb} , i_{Lc} , and switching signal of S_1 obtained from the proposed method according to clamping angles (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (SVPWM) (b) $\theta_a = 30^\circ$, $\theta_b = \theta_c = 0^\circ$ (c) $\theta_a = 60^\circ$, $\theta_b = \theta_c = 0^\circ$.

Figure 15 represents the experimental results of the a -phase load current, switching signal of S_1 and v_{ra_hy} obtained from the proposed method according to clamping angles. Figure 15 indicates that the regions operating with SVPWM and GDPWM differ according to the clamping angle. In Figure 15a, where the clamping angle of all phases is 0° , the inverter operates as SVPWM in all regions. However, in Figure 15b, where the clamping angle of all phases is 60° , the inverter operates as GDPWM in all regions. On the other hand, in Figure 15c,d, the a -phase clamping angles are 30° and 60° , respectively. Therefore, the region operating with GDPWM is larger in Figure 15d than in Figure 15c. In the clamping region, v_{ra_hy} is fixed at $V_{dc}/2$ or $-V_{dc}/2$ to halt the switching operation.

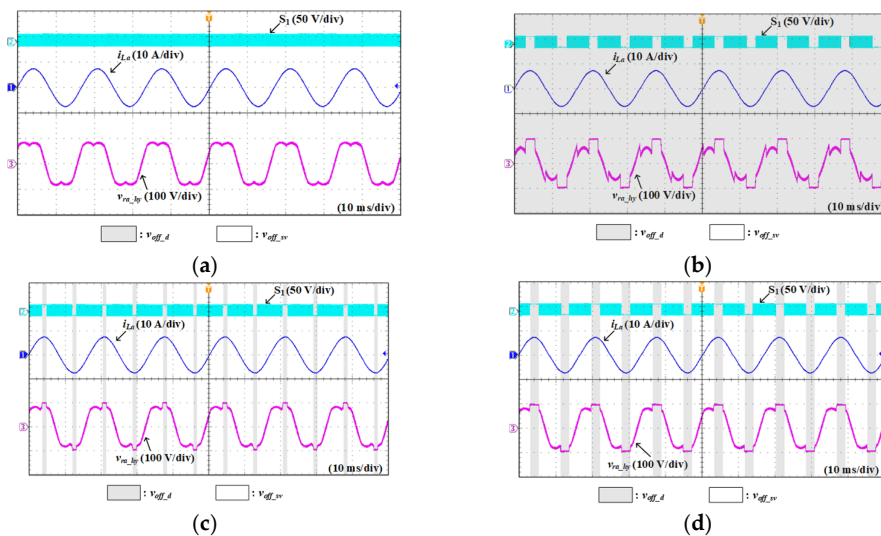


Figure 15. Experimental results of i_{La} , switching signal of S_1 , and v_{ra_hy} obtained from the proposed method according to clamping angles (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (SVPWM) (b) $\theta_a = \theta_b = \theta_c = 60^\circ$ (GDPWM) (c) $\theta_a = 30^\circ$, $\theta_b = \theta_c = 0^\circ$ (d) $\theta_a = 60^\circ$, $\theta_b = \theta_c = 0^\circ$.

Figure 16 represents the experimental results of i_{La} , switching signal of S_1 and v_{off_hy} obtained from the proposed method according to clamping angles. Similar to Figure 15, Figure 16 demonstrates that the regions operating with SVPWM and GDPWM differ according to the clamping angle. In Figure 16a, where the clamping angles of all phases are 0° , v_{off_hy} is the same as the offset voltage for SVPWM. In addition, in Figure 16b, where the clamping angles of all phases are 60° , v_{off_hy} is the same as the offset voltage for GDPWM. Meanwhile, in Figure 16c,d, the offset voltage for GDPWM is used in the clamping region of a -phase and the offset voltage for SVPWM is used in the non-clamping region.

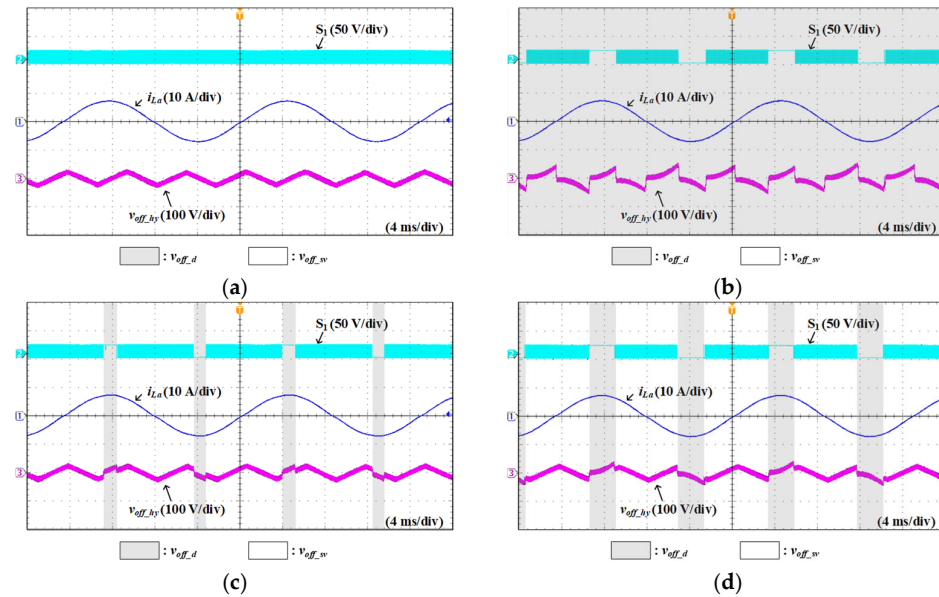


Figure 16. Experimental results of i_{La} , switching signal of S_1 , and v_{off_hy} obtained from the proposed method according to clamping angles (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (SVPWM) (b) $\theta_a = \theta_b = \theta_c = 60^\circ$ (GDPWM) (c) $\theta_a = 30^\circ$, $\theta_b = \theta_c = 0^\circ$ (d) $\theta_a = 60^\circ$, $\theta_b = \theta_c = 0^\circ$.

Figure 17 shows the switching frequencies of each phase when the a -phase clamping angle changes while the b - and c -phase clamping angles are set to 0° . The results in Figure 17 were obtained from the experiment. Similar to the previous simulation results, it can be confirmed in the experiment that only the switching frequency of the a -phase can be diminished independently while maintaining the b -phase and c -phase switching frequencies. Therefore, Figures 11 and 17 indicate that the switching frequency of the phase having the shortest lifespan can be diminished without affecting the switching frequency of other phases by using the proposed hybrid offset voltage.

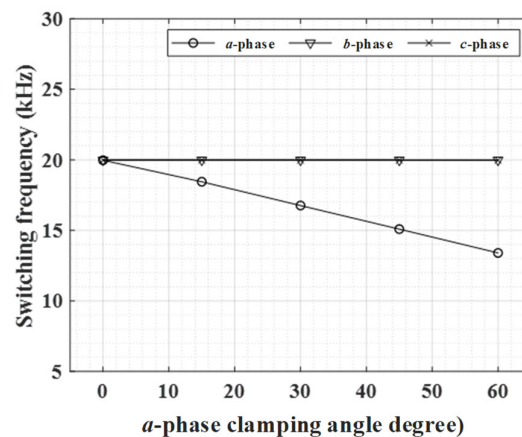


Figure 17. Switching frequencies of each phase according to a -phase clamping angle in $\theta_b = \theta_c = 0^\circ$ (obtained from the experiment).

In this section, the ability to regulate each phase switching frequency of the proposed method was verified by experiments. Experiment results demonstrate that the switching frequency can be independently controlled according to the clamping angle of each phase as in the simulation and that the proposed hybrid offset voltage is calculated as the offset voltage for SVPWM or GDPWM according to the clamping region.

6. Analysis of Lifetime Extension Effect of Proposed Technique

This section verifies the effect of the proposed lifetime extension technique. To do this, it is analyzed how the lifespan of the inverter changes when the switch ages. As mentioned earlier, the lifespan of an inverter is the same as the lifespan of elements with the shortest lifespan. The switching device lifetime is judged to be the shortest [5], so in this paper, the inverter lifetime is estimated from the switching device lifetime. The lifetime of a SiC MOSFET is expressed as Equation (7) [6,24]. It should be noted that

$$N_f = A \Delta T_j^{\beta_1} e^{\frac{\beta_2}{T_{jmin} + 273}} t_{on}^{\beta_3} i_B^{\beta_4} V_c^{\beta_5} d_b^{\beta_6}. \quad (7)$$

In Equation (7), N_f denotes the number of cycles where the switching device fails. Additionally, d_b , V_c , i_B and t_{on} represent bond wire diameter, voltage rating, current per bond and heating time, respectively. Moreover, T_j is the junction temperature. In addition, ΔT_j and T_{jmin} denote the junction temperature variation and the minimum of the junction temperature in Kelvin degrees, respectively. Without information on i_B and d_b , it can be assumed to be 10 A and 400 μm , respectively [25]. V_c is a value obtained by dividing the rated voltage of the switching device by 100. Since the rated voltage of the SiC MOSFET used in this paper is 650 V, V_c becomes 6.5. t_{on} depends on the mission profile. Since the duty of the mission profile used in this paper is 0.5 and the frequency is 0.3 Hz, t_{on} is 1.66 s. Table 3 summarizes the parameters of Equation (7) used in this paper.

Table 3. Parameter in Equation (7).

Parameters	Value
A	9.3×10^{14}
β_1	−4.416
β_2	1285
β_3	−0.463
β_4	−0.716
β_5	−0.761
β_6	−0.5
t_{on} (s)	1.66
i_B (A)	10
V_c (V)	6.5
d_b (μm)	400

As shown in Equation (7), N_f can be calculated only when T_j is known. In this paper, T_j is estimated by the Foster thermal model and losses of SiC MOSFET. The lifetime of the SiC MOSFET and the inverter is calculated through the junction temperature.

6.1. Foster Thermal Model

The Foster thermal model of SCT3080AL is expressed in Figure 18 and Table 4. In Figure 18, P_{tr} is the total loss of the transistor. The case temperature is represented by T_c . In this paper, T_c is assumed to be 50 °C.

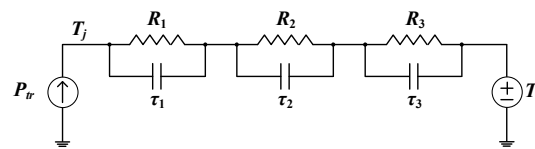


Figure 18. Foster thermal model.

Table 4. Parameter in Foster thermal model of SCT3080AL.

R1 (K/W)	R2 (K/W)	R3 (K/W)	τ_1 (s)	τ_2 (s)	τ_3 (s)
0.092	0.721	0.068	0.00008	0.00473	0.00566

6.2. Loss of Fresh and Aging SiC Mosfet

To calculate T_j using the Foster thermal model in Figure 18, the transistor losses must be known. To this end, the electrical characteristics of fresh and aged SiC MOSFETs were measured through a double pulse test. Aged SiC MOSFET was obtained by accelerated aging stress with a high electric field. The SiC MOSFET used for characteristic measurement is SCT3080AL.

Figure 19 compares electrical characteristics between fresh and aged SiC MOSFETs. In Figure 19, V_{ds} , I_{ds} , E_{on} , E_{off} , V_F , I_F and E_{rr} are drain-source voltage, drain-source current, transistor turn-on energy, transistor turn-off energy, forward diode voltage, diode current and diode reverse recovery current, respectively. Figure 19 indicates that as the SiC MOSFET, SCT3080AL, ages, all electrical characteristics increase except turn-off energy. In addition, the turn-off energy is slightly reduced compared to before aging. Using the switching characteristics of Figure 19, the loss of the switching device was calculated using PSIM. Losses were calculated in Table 5.

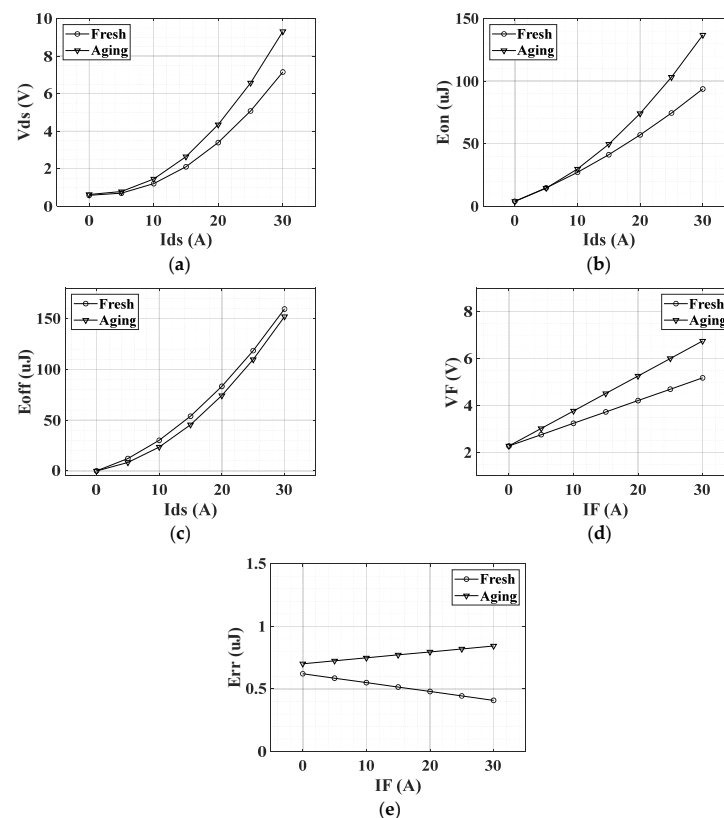


Figure 19. Comparison of electrical characteristics between fresh and aged SiC MOSFETs (a) V_{ds} versus I_{ds} curve (b) E_{on} versus I_{ds} curve (c) E_{off} versus I_{ds} curve (d) V_F versus I_F curve (e) E_{rr} versus I_F curve.

Table 5. Parameter used in loss calculation.

Parameters	Value
L	10 mH
R	15 Ω
C_{dc}	1100 μ F
V_{dc}	1000 V
i_{Lpeak}	25 A
Frequency of reference load current	60 Hz
Carrier frequency	50 kHz

Figure 20 shows loss distributions of switching devices ($S_1, S_3, S_5, S_4, S_6, S_2$) according to clamping angle when a -phase switches in the inverter are aged. In Figure 20, PT_{con} , PT_{sw} , PD_{con} and PD_{sw} mean transistor conduction loss, transistor switching loss, diode conduction loss and diode switching loss, respectively. It should be noted that PD_{sw} , known as reverse recovery loss, appears when the diode changes from the forward conduction phase to the reverse conduction phase. For SiC MOSFET, the reverse recovery loss is negligible. To calculate the loss of a -phase switches, the electrical characteristics of the aged SiC MOSFET in Figure 19 were used. In addition, to calculate the loss of b -phase and c -phase switches, the electrical characteristics of the fresh SiC MOSFET in Figure 19 were used.

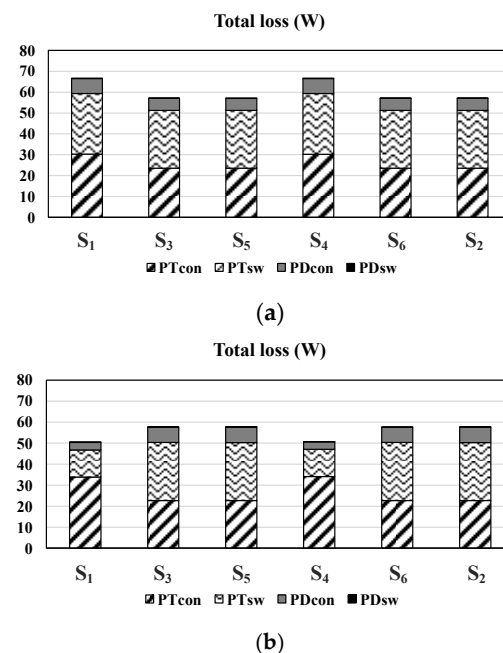
**Figure 20.** Loss distributions of switching devices ($S_1, S_3, S_5, S_4, S_6, S_2$) according to clamping angle when a -phase switches in the inverter are aged (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (b) $\theta_a = 60^\circ, \theta_b = \theta_c = 0^\circ$.

Figure 20a shows loss distributions when all clamping angles are 0° . As shown in Figure 20a, due to the aged a -phase switches, all four types of losses of the a -phase devices, S_1 and S_4 , are larger than the b -phase and c -phase devices. However, in Figure 20b, the loss distribution when the a -phase clamping angle is set to 60° , demonstrates that the loss of S_1 and S_4 is diminished by the proposed method. Therefore, Figure 20 confirms that the proposed technique can decrease the loss of the switching devices having the shortest lifetime.

6.3. Lifetime Estimation Using Junction Temperature

As mentioned earlier, the junction temperature is required for calculating the inverter lifetime. The Foster thermal model and the losses of the switching device are used to calculate T_j . In this subsection, using the simulation, the inverter lifetime is estimated by calculating T_j when the a -phase of the three-phase inverter is aged. Moreover, the expected lifetime extension of the inverter when applying the proposed technique is examined.

For inverter lifetime estimation, a mission profile was used to change the output power from 14 kW to 8 kW. The period of the mission profile used was 3.33 s. It operates at 14 kW for 1.67 s and 8 kW for the remaining 1.67 s. The switching device lifetime becomes shorter as the change in T_j rises. Therefore, to effectively reduce the change in the junction temperature, the proposed method was applied when the output was 14 kW. In addition, SVPWM was applied when the output was 8 kW.

Figure 21 shows transistor junction temperatures according to clamping angle when a -phase switches are aged and other-phase switches are fresh. In Figure 21, $T_{j(Ty)}$ is the transistor junction temperature of S_y ($y = 1, 2, 3, 4, 5, 6$). Figure 21a represents transistor junction temperatures in $\theta_a = \theta_b = \theta_c = 0^\circ$. Moreover, Figure 21b shows the transistor junction temperature in $\theta_a = 60^\circ$ and $\theta_b = \theta_c = 0^\circ$. Figure 21a indicates that ΔT_j and T_{jmin} of a -phase switches are larger than those of other phase switches. This is because, as shown in Figure 20a, the losses of S_1 and S_4 are greater than that of the other fresh phase switches. ΔT_j of S_1 , which is the a -phase upper switch, is 24.8°C and ΔT_j of S_3 is 19.8°C . However, Figure 21b demonstrates that thanks to the decrease in the a -phase switching operation by the proposed technique, the variation of $T_{j(T1)}$, denoted by $\Delta T_{j(T1)}$, is reduced to 13.7°C . Furthermore, since the other phases do not reduce the switching frequency, there is little change in junction temperature.

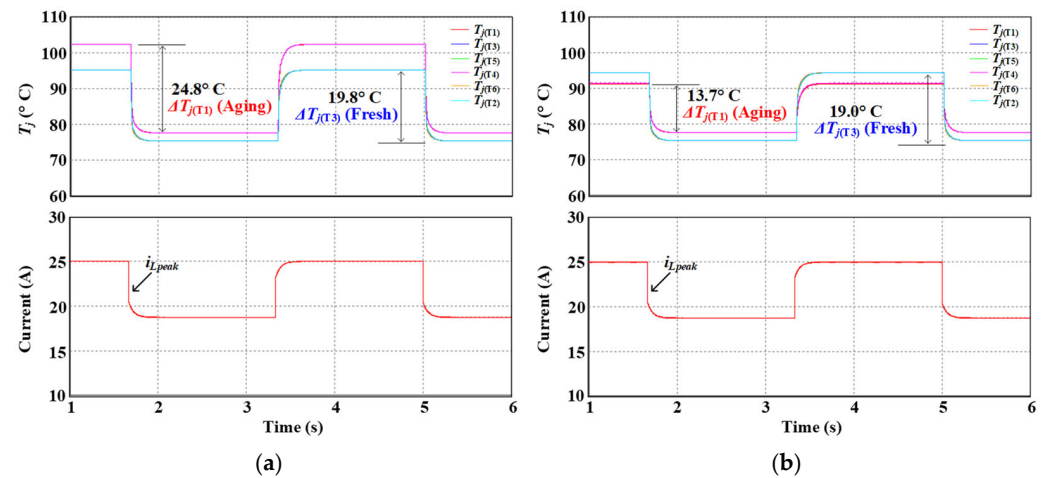


Figure 21. Transistor junction temperatures according to clamping angle when a -phase switches are aged, and other phase switches are fresh (a) $\theta_a = \theta_b = \theta_c = 0^\circ$ (b) $\theta_a = 60^\circ$, $\theta_b = \theta_c = 0^\circ$.

Figure 22 shows ΔT_j of each switch when the a -phase clamping angle changes while the b - and c -phase clamping angles are set to 0° in a three-phase inverter with aged a -phase. Figure 22 shows that as the clamping angle of the a -phase increases, the junction temperature fluctuation of the a -phase switch decreases. In addition, it can be seen that the switches of the remaining phases hardly change.

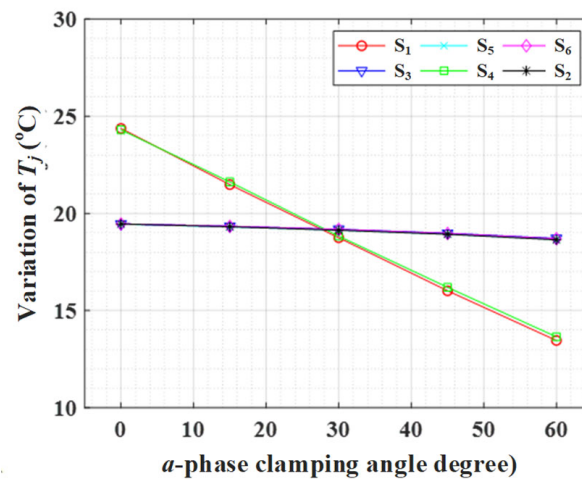


Figure 22. ΔT_j of S_1 , S_3 , S_5 , S_4 , S_6 , and S_2 according to clamping angle when $\theta_b = \theta_c = 0^\circ$.

Equation (7) expresses the lifetime of the switch as the number of cycles. To express this as time, the following Equation (8) is used.

$$L_{sw} = N_f T_{profile} \quad (8)$$

In Equation (8), L_{sw} represents the switching device lifetime. $T_{profile}$ means the period of the mission profile. The $T_{profile}$ used in this paper is 3.33 s. The lifetime of each switch can be estimated using Equations (7) and (8), Table 3 and Figure 22. Figure 23 shows the lifetime of all switches and three-phase inverter according to the a -phase clamping angle. The result in Figure 23 is obtained when the a -phase switches of the three-phase inverter are aged and other phase switches are fresh.

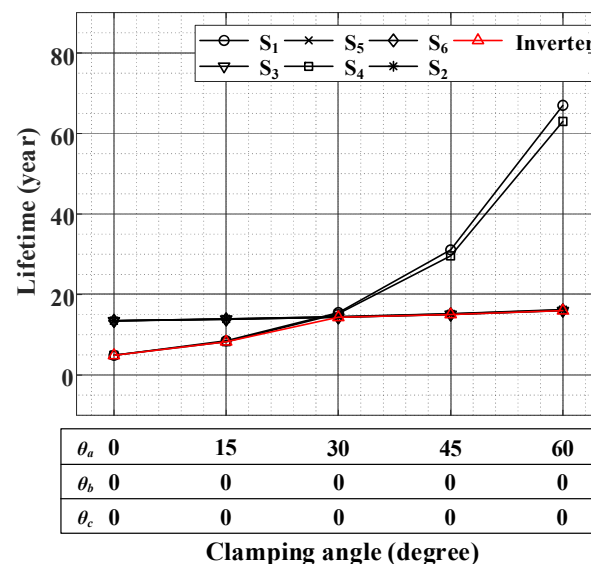


Figure 23. Lifetimes of all switches and three-phase inverter according to the a -phase clamping angle variation.

In Figure 23, the red line represents the three-phase inverter lifetime. The lifespan of the three-phase inverter is determined to be the shortest lifetime among the six switching devices constituting the three-phase inverter. When the a -phase clamping angle is 0° , the lifetimes of the a -phase switches are about 5 years, shorter than the rest of the switches (about 13 years). However, as the a -phase clamping angle increases, the a -phase switch lifetime rises. Eventually, when the clamping angle reaches 30° , the lifetimes of all switches become similar. If the a -clamping angle is raised from 30° , the lifespan of the a -phase switch

increases, but since the overall inverter lifespan is decided by the switching device having the shortest lifespan, the overall inverter lifespan does not show a significant increase after the a -phase clamping angle is 30° .

Figure 24 shows all switches and three-phase inverter lifetimes according to the three-phase clamping angle variation. Unlike Figure 23, in Figure 24, the b - and c -phase clamping angles are set to extend the inverter lifetime even when the a -phase clamping angle is over 30° . As a result, the inverter lifetime increases even when the a -phase clamping angle is more than 30° . Since the proposed technique can independently control the three-phase switching frequencies, the inverter lifetime can be greatly increased by properly setting the three-phase clamping angles, as shown in Figure 24.

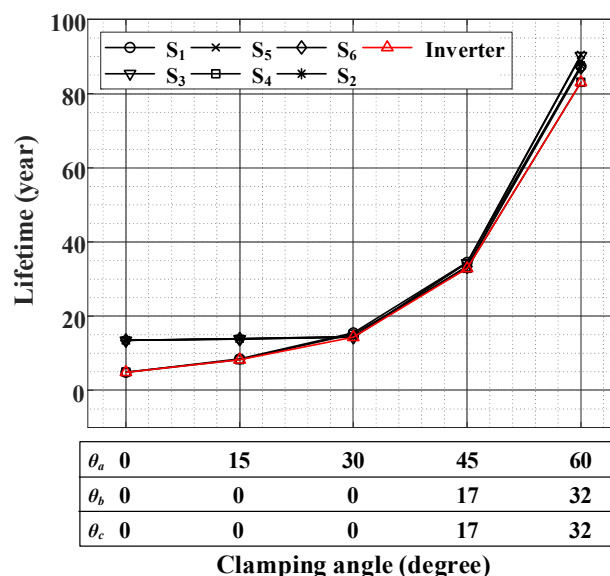


Figure 24. Lifetimes of all switches and three-phase inverter according to the three-phase clamping angle variation.

7. Comparison of Loss and Load Current Quality between Conventional and Proposed Techniques

In this section, the loss and load current quality of the conventional and the proposed techniques are compared. Conventional converter lifetime extension methods are classified into VSFM [7–9] and DPWM-based techniques [10–12]. The VSFM extends the converter lifespan by changing the converter switching frequency. In addition, the DPWM-based technique extends the converter lifespan by changing the width of the clamping region. That is, in the existing techniques, the converter switching frequencies of all phases are equally lowered to extend the converter's lifetime. However, only the switching frequency of the phase having the shortest lifespan can decrease by the proposed method.

There are two major differences between the existing DPWM-based and proposed techniques. The first difference is that the conventional DPWM-based technique adjusts the width of the clamping region of all phases to the same value. However, the proposed technique can adjust the clamping region of each phase differently. This feature improves the load current quality by optimally setting the region where the switching operation stops. The second difference is that the existing DPWM-based technique does not inject offset voltage in the non-clamping region. That is, it is operated with SPWM. However, the proposed technique injects the offset voltage for SVPWM to improve the load current quality in the non-clamping region.

The SVPWM-based VSFM and the DPWM-based lifetime extension technique are used for performance comparison with the proposed technique. The VSFM decreases the switching frequency driven by SVPWM to extend the inverter's lifetime. In addition, the DPWM-based technique extends the inverter lifetime by adjusting the width of the clamping region of all phases to be the same. The loss and load current total harmonic

distortion (THD) of the above two existing techniques and the proposed technique are compared through simulation under the condition of Table 5. In addition, the inverter used for the simulation consists of aged SiC MOSFETs in a -phase and fresh SiC MOSFETs in other phases.

Figure 25 shows the loss comparison between existing techniques (SVPWM, DPWM) and the proposed technique in accordance with the switching frequency reduction in the a -phase. Figure 25a represents the loss of S_1 which is an aged a -phase upper switch. Figure 25b shows the loss of S_4 which is an aged a -phase lower switch. The loss in Figure 25 is the sum of both the transistor and the diode losses. The SVPWM-based VSFM decreases the a -phase switching frequency by reducing all phase switching frequencies of the inverter. In the DPWM-based lifetime extension technique, the a -phase switching operations are diminished by equally reducing the width of the clamping region of all phases. In other words, existing techniques must lower all phase switching frequencies for extending the aged phase lifetime. However, the proposed method can decrease the switching frequency of the aged phase selectively by shortening only the width of the aged phase clamping region thanks to the hybrid offset voltage. Figure 25 shows that all three techniques reduce the loss of a -phase switches by decreasing the switching frequency. In addition, Figure 25 demonstrates that the proposed method can reduce the loss more than the existing methods under the same switching frequency reduction condition. In particular, the reason why the loss of the SVPWM-based technique is greater than that of the existing DPWM-based method and the proposed method at the same switching frequency is that the switching loss can be effectively diminished in the DPWM-based and proposed methods by stopping the switching operation when the current is the largest.

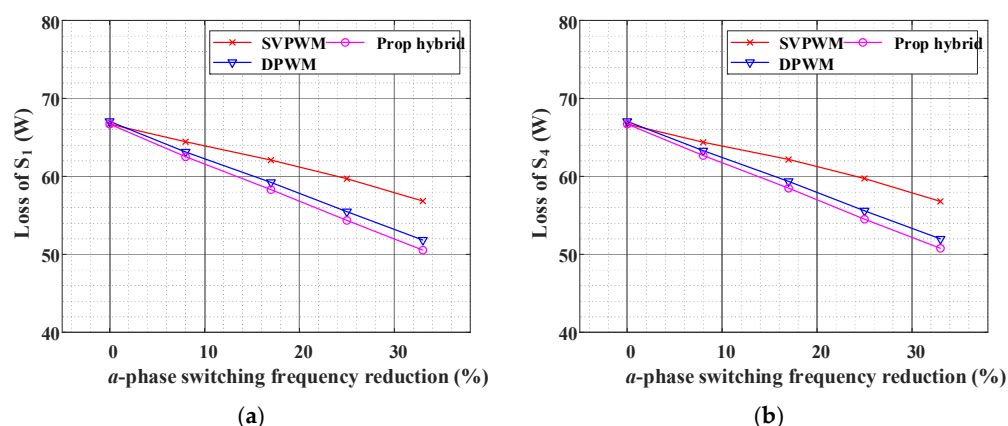


Figure 25. Comparison of loss between existing techniques (SVPWM, DPWM) and the proposed technique in accordance with a -phase switching frequency reduction (a) loss of S_1 (b) loss of S_4 .

On the other hand, the effect of extending the switch lifespan increases as the loss decreases. Therefore, the proposed technique has a greater effect of prolonging the lifespan of the switch than the existing techniques in the same switching operation reduction.

Figure 26 compares the THD of load current between the proposed and the existing methods in accordance with the a -phase switching operation decrease. Figure 25 demonstrates that the existing techniques reduce all phase switching frequencies for lengthening the a -phase lifetime, while the proposed technique only diminishes the switching operation of the aged phase. Figure 26a shows THDs of i_{La} , i_{Lb} and i_{Lc} obtained from the three techniques in accordance with the a -phase switching operation decrease. Figure 26a shows that the three-phase load current THD obtained from the proposed technique is smaller than that of the existing methods. In particular, comparing the THD of i_{La} in the existing DPWM-based technique and the proposed technique indicates that the THD of i_{La} in the proposed technique is small than that in the existing DPWM-based method. This is because, in the conventional DPWM-based technique, the offset voltage is not injected in the non-clamping region, so the inverter operates by SPWM. However, in the proposed technique,

the inverter operates by SVPWM in the non-clamping region. Therefore, the proposed technique has better load current quality than the existing DPWM-based technique even when the width of the clamping region is equally changed. Since the switching operations in the *b*- and *c*-phases are not reduced in the proposed method, the load current THD is small than that of the existing methods.

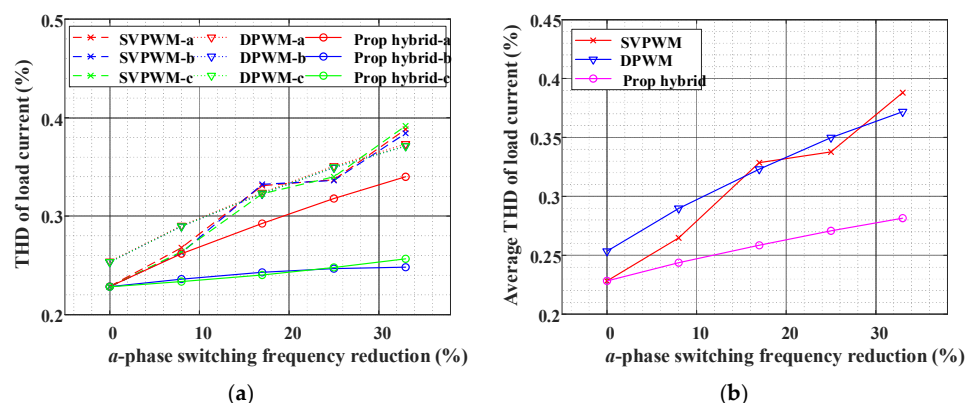


Figure 26. Comparison of load current THD of the proposed method and the existing methods (SVPWM, DPWM) in accordance with *a*-phase switching frequency decrease (a) three-phase load current THD (b) average of load current THD.

Meanwhile, comparing the proposed technique and the existing SVPWM-based method, the THD of the load current in the existing SVPWM-based method and the proposed technique are the same under the condition of not reducing the switching frequency. This is because the proposed scheme operates as SVPWM when the switching operations are not diminished. As the switching frequency reduction increases, the load current THD of the conventional SVPWM-based technique becomes larger than that of the proposed technique. This is because all phase switching frequencies of the inverter are reduced in the conventional SVPWM. The smaller the switching frequency, the worse the load current quality. Figure 26b represents the average THD of i_{La} , i_{Lb} and i_{Lc} in the three techniques in accordance with the switching frequency reduction in the *a*-phase. Similar to the results of Figure 26a above, the proposed method shows that the average THD performance is better than the existing methods. Figure 25 represents that the loss reduction in the proposed technique is greater than that of the conventional methods under the same switching frequency reduction. In addition, Figure 26 shows that the load current THD of the proposed method is smaller than that of the conventional methods under the same switching frequency reduction. Therefore, Figures 25 and 26 indicate that the proposed method can effectively lengthen the inverter's lifetime while improving the inverter load current quality.

8. Conclusions

In this paper, an inverter lifetime extension technique using hybrid offset voltage was proposed. In the proposed technique, the hybrid offset voltage controls each phase switching frequency according to the aging degree of each phase. In the clamping region for reducing the switching frequency, the offset voltage driving GDPWM is used and in the non-clamping region, the offset voltage driving SVPWM was used for good load current quality. GDPWM degrades the load's current quality because it stops the switching operation. In the proposed scheme, the GDPWM is minimally used in the most aged phase to mitigate the degradation of the load current quality due to the stopped switching operation. As a result, compared to the existing techniques, the deterioration of the load current THD can be alleviated and the inverter lifetime can be extended. Simulations and experiments verify the performance of the proposed method.

In the future, the proposed method can be modified and applied to multiphase and multilevel converters. Additionally, a real-time power switch monitoring part can be added

to detect and evaluate the corresponding lifetime. This helps precisely generate a clamping angle for each phase leg depending on its aging condition.

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