



OPEN Effects of channel length on temperature dependence of apparent subthreshold swing in self-aligned top-gate coplanar IGZO thin-film transistors

Chae-Eun Oh^{1,4}, Hwan-Seok Jeong^{2,4}, Su-Hyeon Lee², Hyeon-Woo Lee¹, Dong-Hwi Son¹, Chang-Hyeon Kim¹, Myeong-Ho Kim³, Kyoung-Seok Son³, Jun Hyung Lim³, Sang-Hun Song²✉ & Hyuck-In Kwon¹✉

This study investigates how channel length (L) affects the temperature dependence of the apparent subthreshold swing (SS^*) in self-aligned top-gate coplanar indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs). Our experimental results demonstrate that SS^* increases with temperature for devices with $L = 5\ \mu\text{m}$ and $7\ \mu\text{m}$, yet decreases for devices with $L = 10\ \mu\text{m}$. To elucidate this behavior, we developed a drain current model based on surface potential. Our analysis reveals that variations in the dominant carrier populations (trapped versus free electrons) within the SS^* extraction range dictate the observed temperature dependence of SS^* . Furthermore, the lateral diffusion of donor impurities in our fabricated structures leads to notable differences in the effective channel length across TFTs with varying L s, thereby amplifying these trends. These findings offer crucial insights into the physical mechanisms underlying the channel-length-dependent temperature behavior of SS^* in IGZO TFTs. This understanding is vital for enhancing the stability of active-matrix organic light-emitting diode displays that utilize IGZO TFTs as backplanes.

Keywords SA TG coplanar IGZO TFT, Temperature, Apparent subthreshold swing, Channel length, Stability

Indium–gallium–zinc oxide (IGZO) is a suitable replacement material for amorphous silicon (a-Si) and has been adopted in thin-film transistors (TFTs) owing to its high carrier mobility, low process temperature, and excellent large-area uniformity. Accordingly, IGZO TFTs are currently used in commercial display products such as active-matrix organic light-emitting diode (AMOLED) displays^{1,2}. For high image quality in AMOLED displays, the pixel circuits in the display panel must maintain a constant OLED current because the OLED emits light with an intensity proportional to the OLED current. However, variations in the electrical properties of the driving TFTs degrade the image quality of AMOLED displays³. In particular, variation in the subthreshold swing (SS) of the driving TFTs degrades image quality at low gray levels in AMOLED displays^{4,5}. Because the human eye is more sensitive to image degradation at low gray levels than at high gray levels⁶, it is very important to study the effects of operating conditions on the SS values of driving TFTs in AMOLED displays. Among various operating conditions, operating temperature has been reported to have a strong influence on the SS values of oxide TFTs^{7–9}. However, previous studies have reported inconsistent experimental results regarding the temperature dependence of SS values in oxide TFTs. Most research groups reported an increase in SS values with an increase in operating temperature from 300 to 360 K^{10,11}, whereas a few groups reported a decrease in SS values with increasing temperature in a similar temperature range^{12,13}. Unfortunately, the physical mechanism responsible for these inconsistent results has not yet been identified. Because AMOLED displays operate across a wide range of temperatures, it is crucial to systematically study the temperature dependence of SS values in IGZO TFTs so that consistent image quality can be maintained over a wide temperature range with appropriate compensation methods. In this study, we observed that the channel length (L) of the device can significantly

¹Major in Intelligent Semiconductor Engineering, Chung-Ang University, 84 Heukseok-ro, Dongjak-gu, Seoul, Korea. ²School of Electrical and Electronics Engineering, Chung-Ang University, 84 Heukseok-ro, Dongjak-gu, Seoul, Korea. ³Samsung Display, 162, Nongseo-ro, Giheung-gu, Yongin-si, Gyeonggi-do, Korea. ⁴Chae-Eun Oh and Hwan-Seok Jeong have contributed equally to this work. ✉email: shsong@cau.ac.kr; hyuckin@cau.ac.kr

affect the temperature dependence of the apparent SS (SS^*) in the fabricated IGZO TFTs, where SS^* was defined as the gate voltage (V_G) required to increase the drain current (I_D) from 10^{-12} A to 10^{-11} A at a drain voltage (V_D) of 0.1 V, based on the current range commonly used to extract SS in several previous studies on IGZO TFTs including Refs.^{14,15}. This current range corresponds to the operating current level of AMOLED pixels under low-luminance conditions. To elucidate the origin of this behavior, an I_D model based on the surface potential (ϕ_s) was derived for IGZO TFTs. The development of compact models based on mathematical formulations has been shown to be valuable in describing complex system characteristics^{16,17}. By comparing the calculated and measured I_D characteristics at various temperatures for devices with different L s, the underlying mechanism responsible for the observed phenomena was identified.

Results and discussion

Figure 1 illustrates a schematic cross-section of the fabricated self-aligned top-gate (SA TG) coplanar IGZO TFT. The fabrication process is described in detail in the Methods section. The SA TG coplanar structure is commonly employed in the fabrication of IGZO TFTs for AMOLED applications due to its low parasitic capacitance and excellent process control^{18,19}. Figures 2a–c show the transfer characteristics (V_G versus I_D) of the fabricated SA TG coplanar IGZO TFTs measured at temperatures from 25 °C to 85 °C with $V_D = 0.1$ V. The L was set to (a) 5 μm , (b) 7 μm , and (c) 10 μm , respectively, with the channel width (W) fixed at 3 μm . Transfer curves in Figs. 2a–c are taken from representative devices among five measured samples for each L . All electrical measurements were performed using an Agilent 4156C semiconductor parameter analyzer, with the TFT's source and back gate electrically connected. Temperature-dependent measurements were conducted using a temperature-controlled thermal chuck system, where the devices were allowed to stabilize at each target temperature for at least 5 min before data acquisition. All measurements were performed in the dark. Figures 2a–c show that the transfer curve shifts negatively with a decrease in L . These results are consistent with those in the previous works and the more negative shift of the transfer curves in shorter-channel TFTs was attributed to the higher carrier concentration in the channel region caused by the carrier diffusion from the n^+ -doped source/drain extension regions¹⁸. Figure 2d summarizes the SS^* values extracted as the inverse slope of the transfer curve ($dV_G/d(\log I_D)$) over the range of 10^{-12} A $< I_D < 10^{-11}$ A, following definitions used in prior studies on IGZO TFTs. The plotted values represent averages over five devices for each L , with vertical error bars indicating ± 1 standard deviation. Figure 2d shows that the average SS^* value obtained from the IGZO TFTs with $L = 5$ and 7 μm increases with an increase in the temperature from 25 to 85 °C (from 0.137 to 0.164 V/decade for TFT with $L = 5$ μm and from 0.144 to 0.152 V/decade for TFT with $L = 7$ μm), whereas that obtained from the IGZO TFT with $L = 10$ μm slightly decreases from 0.181 to 0.172 V/decade with an increase in the temperature from 25 to 85 °C. The results Fig. 2d clearly show that the channel length of the device strongly affects the temperature dependence of SS^* in the fabricated SA TG coplanar IGZO TFTs.

To elucidate the origin of this behavior, an I_D model based on ϕ_s was developed for IGZO TFTs. Figure 3a illustrates the energy band diagram along the depth direction of the IGZO thin film. In the diagram, q is the elementary charge, t_s is the IGZO film thickness, x is the position along the vertical direction measured from the IGZO/gate insulator interface, y is the coordinate along the lateral direction from the source, ϕ_{F0} is the bulk-Fermi potential, $\phi(x)$ is the electric potential along the depth direction, E_{F0} is the Fermi level at the flat-band condition, E_C is the conduction band minimum, E_V is the valence band maximum, $V_{CH}(y)$ is the potential difference [i.e., describing the electron quasi-Fermi level E_{Fn} lowered by $qV_{CH}(y)$ due drain voltage V_D along the channel length direction]. In this study, the subgap states near E_C are assumed to consist of the acceptor-like trap states that are exponentially distributed in energy in IGZO^{12,13}. These trap states originate from structural disorder in the amorphous IGZO matrix, such as variations in metal–oxygen bonding and oxygen vacancy-related defects, which create localized states near E_C ^{20,21}. Figure 3b shows a schematic illustration of the subgap density of acceptor-like states over the bandgap near E_C ($g(E)$) in the model²²:

$$g(E) = N_T \exp\left(\frac{E - E_C}{kT_T}\right), \quad (1)$$

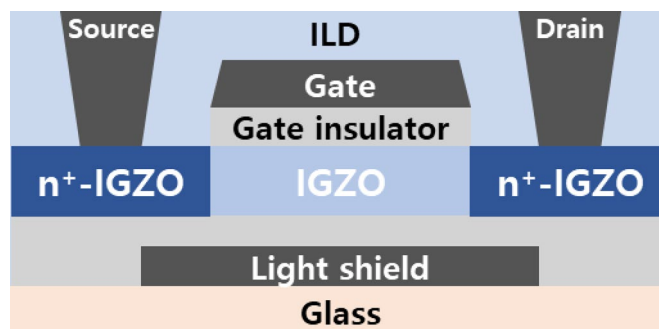


Fig. 1. Schematic cross-section of the fabricated SA TG coplanar IGZO TFTs.

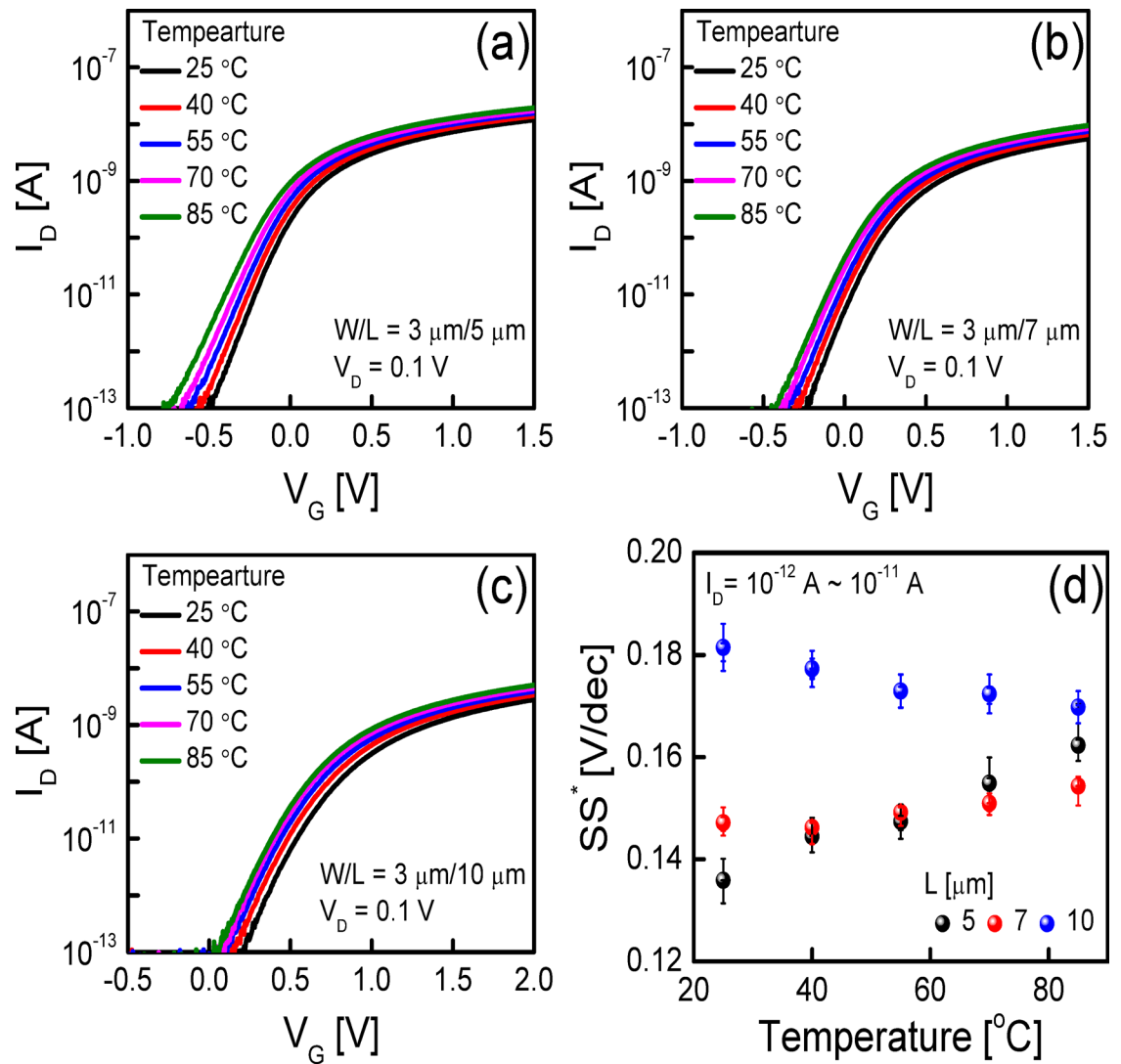


Fig. 2. Representative transfer characteristics of the fabricated SA TG coplanar IGZO TFTs with L of (a) 5 μm , (b) 7 μm , and (c) 10 μm , measured at different temperatures (25–85 $^{\circ}\text{C}$) at $V_D = 0.1\text{ V}$. The W was fixed at 3 μm in all devices. (d) SS^* values extracted from the fabricated IGZO TFTs with L of 5 μm , 7 μm , and 10 μm at different temperatures, where each value represents the average of five devices, and the vertical error bars indicate ± 1 standard deviation.

where E is the electron energy, N_T is the density of trap states extrapolated to E_C , k is the Boltzmann constant, and kT_T is the characteristic energy of the acceptor-like states. Based on the gradual channel approximation, the one-dimensional Poisson equation along the channel depth (x) can be expressed as²³

$$\frac{d^2\varphi(x)}{dx^2} = \frac{q}{\varepsilon_S} (n_{Free}(x) + n_{Trap}(x)), \quad (2)$$

where ε_S is the IGZO permittivity. Here, $n_{Trap}(x)$ and $n_{Free}(x)$ represent the densities of trapped electrons in localized acceptor-like trap states and free electrons, respectively, and can be expressed as^{24,25}

$$n_{Trap}(x) \approx N_T kT_T \exp \left[\frac{E_{F0} - E_C + q\varphi(x) - qV_{CH}}{kT_T} \right], \quad (3)$$

$$n_{Free}(x) \approx N_C \exp \left[\frac{E_{F0} - E_C + q\varphi(x) - qV_{CH}}{kT} \right], \quad (4)$$

where N_C is the effective density of states of free electrons and T is the temperature. Then, the electric field inside the IGZO thin film ($E_{IGZO}(x)$), which is defined as Eq. (5),

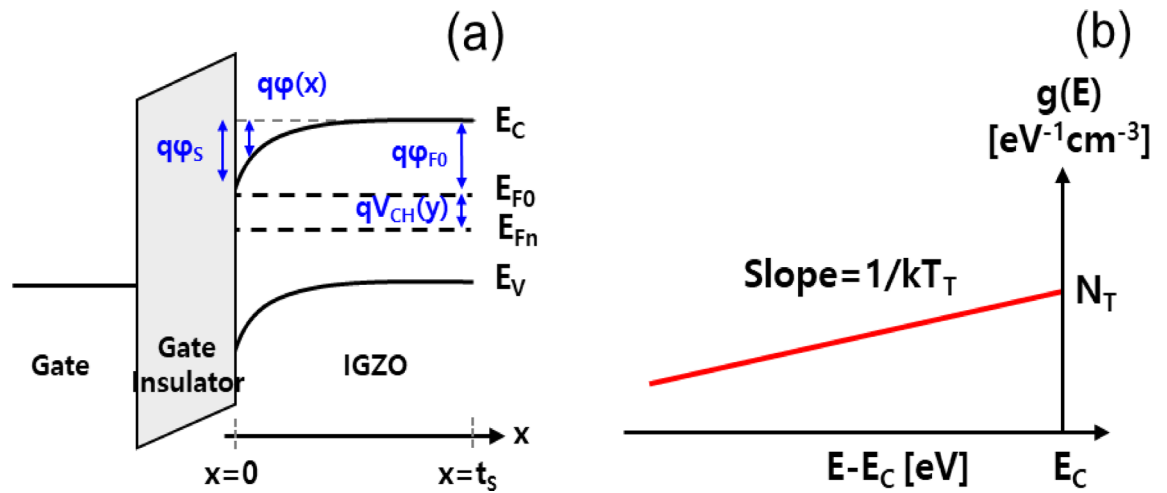


Fig. 3. (a) Energy band diagram along the thin-film depth direction of the SA TG coplanar IGZO TFT. (b) Schematic illustration of the subgap density of acceptor-like states over the bandgap near E_C ($g(E)$) in IGZO.

$$E_{IGZO}(x) = -\frac{d\varphi(x)}{dx} \quad (5)$$

can be solved by multiplying both sides of Eq. (2) by $2\varphi(x)/dx$ and then integrating over x . Together with the boundary conditions $\varphi(t_{\zeta})=d\varphi(t_{\zeta})/dx=0$, $d\varphi(x)/dx$ can be solved as Eq. (6)¹¹.

$$\begin{aligned} \int_{t_S}^x 2 \frac{d\varphi(x)}{dx} \cdot \frac{d^2\varphi(x)}{dx^2} dx &= \int_{t_S}^x \frac{d}{dx} \left(\frac{d\varphi(x)}{dx} \right)^2 dx = \left(\frac{d\varphi(x)}{dx} \right)^2 \\ \int_{t_S}^x \frac{2q}{\varepsilon_S} \left(\frac{d\varphi(x)}{dx} \right) [n_{Free}(x) + n_{Trap}(x)] dx &= \frac{2q}{\varepsilon_S} \int_0^{\varphi(x)} [n_{Free}(x) + n_{Trap}(x)] d\varphi(x) \end{aligned} \quad (6)$$

By using Eq. (5) and substituting Eqs. (3) and (4) into Eq. (6), the surface electric field $E_s = E_{\text{IGZO}}(x=0)$ can be expressed as

$$\begin{aligned}
E_S &= \sqrt{\frac{2q}{\varepsilon_S} \int_0^{\varphi_S} [n_{Free}(x) + n_{Trap}(x)] d\varphi(x)} \\
&= \sqrt{\frac{2N_T (kT)^2}{\varepsilon_S} \exp\left(\frac{E_{F0} - E_C + q\varphi_S - qV_{CH}}{kT}\right) + \frac{2N_C kT}{\varepsilon_S} \exp\left(\frac{E_{F0} - E_C + q\varphi_S - qV_{CH}}{kT}\right)}
\end{aligned} \tag{7}$$

Using Gauss's law with Eq. (7),

$$\begin{aligned} \varepsilon_S E_S &= C_{OX} (V_G - V_{FB} - \varphi_S - V_{CH}) \\ &= \sqrt{2\varepsilon_S N_T (kT_T)^2} \exp\left(\frac{E_{F0} - E_C + q\varphi_S - qV_{CH}}{kT_T}\right) + 2\varepsilon_S N_C kT \exp\left(\frac{E_{F0} - E_C + q\varphi_S - qV_{CH}}{kT}\right), \end{aligned} \quad (8)$$

where V_{FB} and C_{OX} denote the flat-band voltage and gate insulator capacitance per unit area, respectively. From Eq. (8), ϕ_s can be obtained as a function of V_G :

Most acceptor-like trap states below E_{Fn} are occupied by electrons at low temperatures ($kT \approx 0$ K) in IGZO; however, electrons can be released by thermal excitation from the occupied trap states into the conduction band and can contribute to I_{D} with an increase in temperature^{26,27}. In IGZO TFTs, at low V_{GS} , $n_{\text{Trap}}(x)$ exceeds $n_{\text{Free}}(x)$, so, $n_{\text{Trap}}(x) + n_{\text{Free}}(x) \sim n_{\text{Trap}}(x)$, whereas at high V_{GS} , $n_{\text{Trap}}(x)$ is smaller than $n_{\text{Free}}(x)$, so, $n_{\text{Trap}}(x) + n_{\text{Free}}(x) \sim n_{\text{Free}}(x)$. Therefore, at each condition, $E_{\text{IGZO}}(x)$ in Eq. (6) can be simplified as Eq. (9) and (10) when $n_{\text{Trap}}(x) > n_{\text{Free}}(x)$ and $n_{\text{Trap}}(x) < n_{\text{Free}}(x)$, respectively.

$$E_{IGZO}(x) \approx \sqrt{\frac{2N_T(kT_T)^2}{\varepsilon_S}} \exp\left(\frac{E_{F0} - E_C + q\varphi_s - qV_{CH}}{kT_T}\right), \quad (n_{Trap}(x) \gg n_{Free}(x)) \quad (9)$$

$$E_{IGZO}(x) \approx \sqrt{\frac{2N_C kT}{\varepsilon_S}} \exp\left(\frac{E_{F0} - E_C + q\varphi_s - qV_{CH}}{kT}\right), \quad (n_{Trap}(x) \ll n_{Free}(x)) \quad (10)$$

Considering that I_D in IGZO TFTs can be expressed as²⁷

$$I_D = q \frac{W}{L} \mu_{FE} \int_0^{V_D} \int_0^{t_S} n_{Free}(\varphi, V_{CH}) dx dV_{CH} = q \frac{W}{L} \mu_{FE} \int_0^{V_D} \int_0^{\varphi_S} \frac{n_{Free}(\varphi, V_{CH})}{E_{IGZO}(x)} d\varphi dV_{CH} \quad (11)$$

I_D can be simplified under the conditions of $n_{Trap}(x) > n_{Free}(x)$ and $n_{Trap}(x) < n_{Free}(x)$, respectively, as follows:

$$I_{D1} = q \frac{W}{L} \mu_{FE} \frac{\sqrt{\varepsilon_S} N_C}{\sqrt{2N_T(kT_T)^2}} \exp\left((E_{F0} - E_C + q\varphi_s) \left(\frac{1}{kT} - \frac{1}{2kT_T}\right)\right) \left(\frac{1}{kT} - \frac{1}{2kT_T}\right)^{-2} \\ (1 - \exp(-qV_D \left(\frac{1}{kT} - \frac{1}{2kT_T}\right))) \approx q \frac{W}{L} \mu_{FE} \frac{\sqrt{\varepsilon_S} N_C}{\sqrt{2N_T(kT_T)^2}} \exp\left((E_{F0} - E_C + q\varphi_s) \left(\frac{1}{kT} - \frac{1}{2kT_T}\right)\right) \left(\frac{1}{kT} - \frac{1}{2kT_T}\right)^{-2}, \quad (12) \\ V_D > 3kT, \quad (n_{Trap}(x) \gg n_{Free}(x))$$

$$I_{D2} = q \frac{W}{L} \mu_{FE} \int_0^{V_D} \sqrt{2\varepsilon_S N_C kT} \exp\left(\frac{E_{F0} - E_C + q\varphi_s - qV_{CH}}{kT}\right) dV_{CH} \\ = q \frac{W}{L} \mu_{FE} \int_0^{V_D} C_{OX} (V_G - V_{FB} - \varphi_s - V_{CH}) dV_{CH} \\ = q \frac{W}{L} \mu_{FE} C_{OX} \left(V_G - V_{FB} - \varphi_s - \frac{1}{2}V_D\right) V_D, \quad (n_{Trap}(x) \ll n_{Free}(x)) \quad (13)$$

where, the boundary conditions for V_{CH} are $V_{CH}(y=0)=0$ and $V_{CH}(y=L)=V_D$, respectively. In Eqs. (12) and (13), μ_{FE} ($=P_{TLC}\mu_{per}$) is the field-effect mobility determined based on the trap-limited and percolation conduction mechanisms, where the effect of trap-limited conduction can be considered as ratio of n_{Free} and n_{Trap} , yielding $P_{TLC} = n_{Free}/(n_{Free} + n_{Trap})$. μ_{per} is the percolation mobility of²⁸

$$\mu_{per} = \mu_0 \exp\left(-\frac{q(\phi_{B0} - \Delta\phi_B)}{kT} + \frac{(q\sigma_{B0})^2}{2(kT)^2}\right) = \mu_0 * \exp\left(\frac{\gamma_B \Delta E_F}{kT} - q\phi_{B0}\right), \quad (14)$$

where $\mu_0^* = \mu_0 \exp[-q\phi_{B0}/kT + (q\sigma_{B0})^2/(kT)^2]$ is an effective band mobility. Here, percolation conduction, governed by potential barriers located above E_C , can be modeled as a mobility scaled from the intrinsic band mobility (μ_0), under the assumption of a Gaussian random distribution of potential barriers characterized by a mean value (ϕ_{B0}) and variance (σ_{B0}). ϕ_{B0} can be lowered by $\Delta\phi_{B0}$ due to thermally excited electrons, which is influenced by the shift in the Fermi level (ΔE_F). The reduction factor γ_B is defined as $\gamma_B = (D_B - W_B)/D_B$, where D_B and W_B represent the spatial distance and width of the potential barriers in IGZO, respectively. Equations (12) and (13) can be combined as a total I_D using a harmonic average²⁹

$$I_D = \left(\frac{1}{(I_{D1})^m} + \frac{1}{(I_{D2})^m}\right)^{-\frac{1}{m}}, \quad (15)$$

where m is the fitting coefficient.

Figure 4a shows the n_{Free} , n_{Trap} , and n_{Tot} ($=n_{Free} + n_{Trap}$) calculated as a function of V_G using Eqs. (3) and (4) at 25 °C, and Figs. 4b and c show the transfer curves calculated using Eqs. (12) and (13) at different temperatures ranging from 25 °C to 85 °C when $n_{Tot} \sim n_{Trap}$ (Fig. 4b) and $n_{Tot} \sim n_{Free}$ (Fig. 4c), respectively. The model parameters used to calculate n_{Free} , n_{Trap} and each transfer curves are shown in Table 1. From the calculation results in Figs. 4b and c, it is observed that when $n_{Tot} \sim n_{Trap}$ (at low V_G s), the V_G range required to achieve the same I_D variation increases with temperature, whereas when $n_{Tot} \sim n_{Free}$ (at high V_G s), the required V_G range decreases as temperature increases.

Figures 5a–c show the transfer curves calculated using Eq. (15) at temperatures ranging from 25 to 85 °C for IGZO TFTs with $W/L=0.1$ (Fig. 5a), 1 (Fig. 5b), and 10 (Fig. 5c), respectively. Figure 5d summarizes the SS^* values extracted from each IGZO TFT at various temperatures within the same range. It is observed in Fig. 5d that the SS^* value increases with increasing temperature for $W/L=10$, whereas it decreases with increasing temperature for $W/L=0.1$. Based on the calculation results shown in Fig. 4, this behavior can be attributed to the fact that, for the device with $W/L=10$, the I_D region used to extract the SS^* value satisfies the $n_{Tot} \sim n_{Trap}$ condition, while for the device with $W/L=0.1$, the same current range satisfies the $n_{Tot} \sim n_{Free}$ condition. The calculation results presented in Fig. 5 exhibit a consistent trend with the experimental results shown in Fig. 2, where the SS^* values

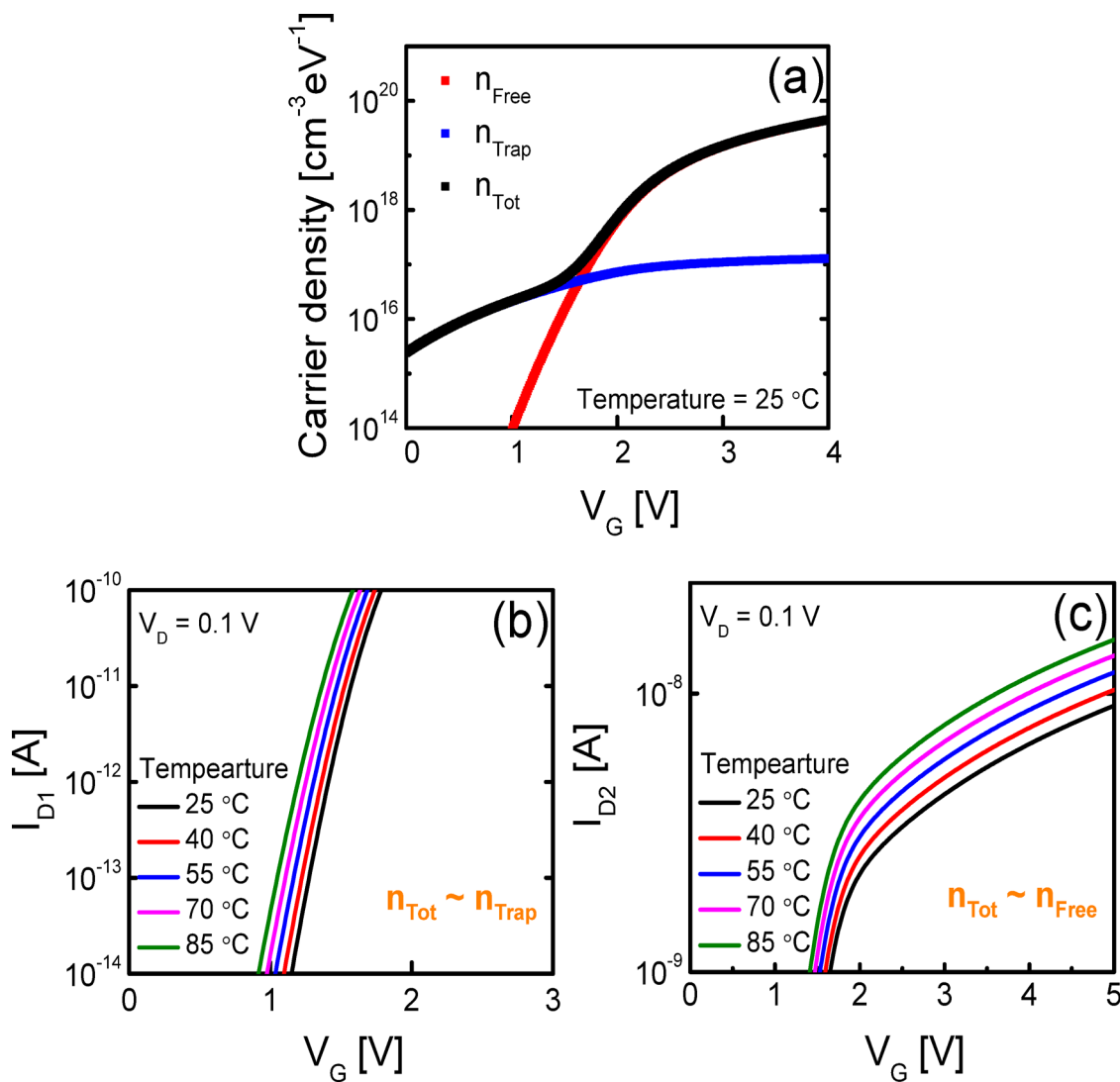


Fig. 4. (a) n_{Free} , n_{Trap} , and n_{Tot} ($=n_{\text{Free}} + n_{\text{Trap}}$) calculated as a function of V_G at 25 °C. Transfer curves calculated using the derived model at different temperatures ranging from 25 to 85 °C when (b) $n_{\text{Tot}} \sim n_{\text{Trap}}$ and (c) $n_{\text{Tot}} \sim n_{\text{Free}}$.

Parameter	Quantity	value
W/L	Channel width/channel length	5
ϵ_{OX}	Permittivity of gate insulator	4
t_{OX}	Thickness of Insulator	$120 \times 10^{-7} \text{ cm}$
N_C	Effective density of states of free carriers	$5 \times 10^{18} \text{ cm}^{-3}$
ϵ_S	Permittivity of IGZO	10
μ_{band}^*	Band mobility	$20 \text{ cm}^2/\text{Vs}$
$E_{\text{F0}} - E_C$	Activation energy at flat band conditions	-0.3 eV
N_T	Density of trap states extrapolated to E_C	$5 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$
kT_T	Characteristic energy for acceptor-like tail states	0.19 eV
$\gamma_B \phi_{B0}$	Spatial coherence ratio of the potential barriers	0.004 eV
m	fitting coefficient	1

Table 1. Model parameters used to calculate n_{Free} , n_{Trap} , and transfer curves of the IGZO TFTs in this study.

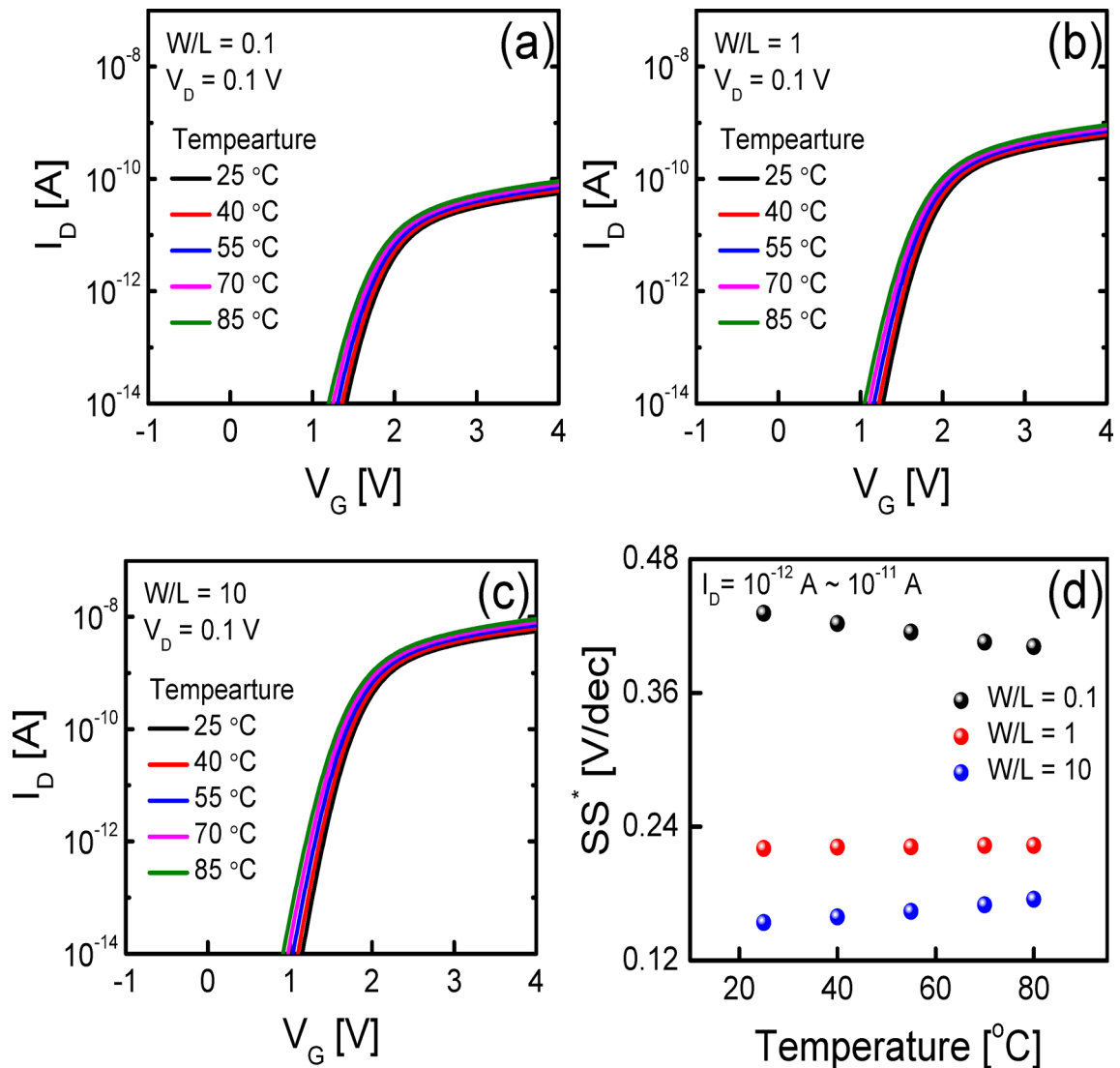


Fig. 5. Full range transfer characteristics calculated using the derived model for IGZO TFTs with W/L ratios of (a) 0.1, (b) 1, and (c) 10, over a temperature range of 25 °C to 85 °C. (d) Extracted SS^* values for each IGZO TFT at various temperatures within the same range.

obtained from fabricated IGZO TFTs with $L=5$ and $7\ \mu\text{m}$ increase with increasing temperature, whereas the value obtained from the IGZO TFT with $L=10\ \mu\text{m}$ decreases as the temperature increases.

The results in Figs. 4 and 5 demonstrate that the variation in the temperature dependence of the SS^* with L , observed in Fig. 2, originates from differences in the dominant type of electrons within the I_D range used to extract the SS^* , depending on L . Nevertheless, the significant change in the temperature dependence of the SS^* , despite only a twofold increase in L from 5 to $10\ \mu\text{m}$ in Fig. 2, cannot be fully explained by this interpretation alone. To better understand the phenomenon observed in Fig. 2, we compared the effective channel lengths (L_{eff}) of the fabricated SA TG coplanar IGZO TFTs. As stated, prior research reported that oxygen vacancies or hydrogen atoms diffused from the n^+ -doped source/drain extension regions into the IGZO channel layer during the subsequent annealing process, leading to a reduction in L_{eff} in the SA TG coplanar IGZO TFTs^{30,31}. Figure 6a indicates the schematic plot illustrating the concept of $L_{\text{eff}}(V_{\text{OV}})$ in SA TG coplanar IGZO TFTs, where V_{OV} is the overdrive voltage ($V_{\text{OV}} = V_G - V_T$) and V_T is the threshold voltage. Figure 6b shows the $\Delta L(V_{\text{OV}})$ ($L_{\text{eff}}(V_{\text{OV}}) = L - \Delta L(V_{\text{OV}})$) extracted using the paired V_G -based transmission line method^{18,32}. Considering that the SS^* values were extracted at very low V_{OV} s close to 0 V, the L_{eff} of the $10\ \mu\text{m}$ TFT appears to be at least 5 to 6 times larger than that of the $5\ \mu\text{m}$ TFT in the I_D region used to extract the SS^* value. This is believed to be the reason for the distinct difference observed in the temperature dependence of the SS^* in the fabricated SA TG coplanar IGZO TFTs, despite only a twofold change in L .

Generally, in disordered semiconductor-based TFTs, the subthreshold region is defined as the regime where $n_{\text{Tot}} \sim n_{\text{Trap}}$, and thus the SS is typically extracted from this region³³. However, in the case of IGZO TFTs, the bandgap of IGZO is very large (greater than 3.0 eV)^{34,35}. As a result, the off-currents and small subthreshold currents are often below the detection limit of conventional DC measurement equipment³⁶. Consequently, the

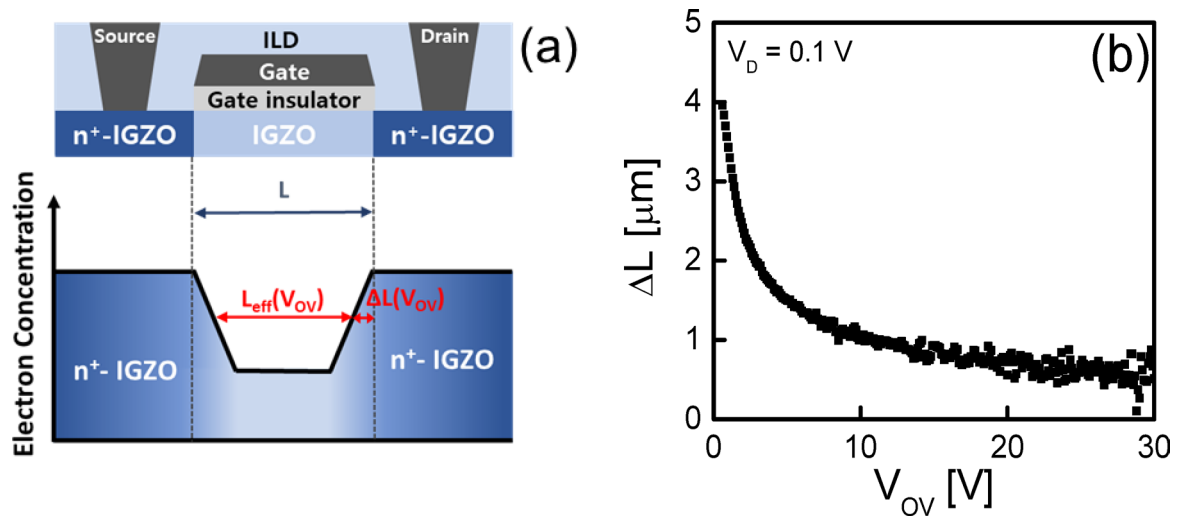


Fig. 6. (a) Schematic plot illustrating the concept of $L_{\text{eff}}(V_{\text{OV}})$ in SA TG coplanar IGZO TFTs. (b) $\Delta L(V_{\text{OV}})$ ($L_{\text{eff}}(V_{\text{OV}}) = L - \Delta L(V_{\text{OV}})$) extracted from the fabricated SA TG coplanar IGZO TFTs using the paired V_G -based transmission line method.

I_D range commonly used for extracting SS in prior studies for IGZO TFTs ($I_D \sim 10^{-13}$ to 10^{-10} A) may correspond to different operating regimes such as $n_{\text{Tot}} \sim n_{\text{Trap}}$, $n_{\text{Tot}} \sim n_{\text{Trap}} + n_{\text{Free}}$ or $n_{\text{Tot}} \sim n_{\text{Free}}$, depending on various factors including the device dimension. This variation is considered to be a major reason for the inconsistent experimental results reported in prior studies regarding the temperature dependence of SS in oxide TFTs.

Conclusion

In this study, we observed that the temperature dependence of SS^* varies with L in SA TG coplanar IGZO TFTs, and investigated the underlying mechanisms. Experimentally, as the temperature increased from 25 to 85 °C, the SS^* increased with temperature for the device with $L = 5 \mu\text{m}$ and $7 \mu\text{m}$ whereas it decreased for devices with $L = 10 \mu\text{m}$. To elucidate the origin of the observed phenomenon, ϕ_s -based I_D modeling was performed for IGZO TFTs. The calculation results revealed that in the $n_{\text{Tot}} \sim n_{\text{Trap}}$ (at low V_G s), the V_G range required to achieve the same I_D variation increases with temperature, whereas in the $n_{\text{Tot}} \sim n_{\text{Free}}$ (at high V_G s), the required V_G range decreases with increasing temperature. Based on the developed model, it was considered that for devices with shorter channel lengths, the SS^* was extracted in the $n_{\text{Tot}} \sim n_{\text{Trap}}$ region, whereas for devices with longer channel lengths, the measurement region corresponded to the $n_{\text{Tot}} \sim n_{\text{Free}}$ region. Furthermore, the lateral diffusion of donor impurities from the source/drain extension regions into the IGZO channel layer in the SA TG coplanar IGZO TFTs is believed to enlarge the difference in L_{eff} compared to the drawn gate length differences. This effect amplifies the variation in the temperature dependence of SS^* even between devices with relatively small differences in drawn gate lengths.

Methods

An Al layer was deposited and patterned on a glass substrate to serve as the back gate electrode, which also functions as a light shield. Subsequently, a 300-nm thick SiO_x layer was deposited as a buffer layer using plasma-enhanced chemical vapor deposition (PECVD) at 350 °C. A 30-nm thick IGZO channel layer (In:Ga:Zn = 1:1:1 atomic percentage) was then deposited via radio-frequency magnetron sputtering, followed by the deposition of a 120-nm thick SiO_x gate insulator using PECVD at 200 °C. A Mo layer was then deposited and patterned to form the gate electrode. After the deposition and patterning of the Mo gate electrode and the SiO_x gate insulator, a SiO_x and SiN_x layer were sequentially deposited as an interlayer dielectric (ILD) using PECVD and patterned to create via holes. The source and drain electrodes, made of Al, were deposited and patterned on the n⁺-doped IGZO source/drain extension regions. In these regions, hydrogen, diffusing from the PECVD-deposited ILD, acts as an electron donor in the IGZO, thus forming the source/drain extension regions. Finally, the TFTs were passivated with a SiO_x layer and thermally annealed at 340 °C to achieve stable and uniform electrical characteristics.

Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

Received: 16 June 2025; Accepted: 29 August 2025

Published online: 06 October 2025

References

- Kim, J. Y., Kim, H., Kim, D. & Jang, H. W. Advancements of Amorphous IGZO-based transistors: Materials, processing, and devices. *ACS Appl. Electron. Mater.* (2025).
- Peng, C., Yang, S., Pan, C., Li, X. & Zhang, J. Effect of two-step annealing on high stability of a-IGZO thin-film transistor. *IEEE Trans. Electron. Dev.* **67**, 4262–4268 (2020).
- Lin, C. L., Chang, W. Y. & Hung, C. C. Compensating pixel circuit driving AMOLED display With a-IGZO TFTs. *IEEE Trans. Electron. Dev.* **34**, 1166–1168 (2013).
- Keum, N. H., Chai, C. C., Hong, S. K. & Kwon, O. K. A compensation method for variations in subthreshold slope and threshold voltage of thin-film transistors for AMOLED displays. *IEEE J. Electron. Dev. Soc.* **7**, 462–469 (2019).
- Zhang, K., Zheng, Y., Dang, P. & Peng, G. The challenge of OLED display quality in low gray scale. in *Proceedings of the International Display Workshops (IDW)* **26**, OLED1–8 (2019).
- Keum, N. H., Hong, S. K. & Kwon, O. K. An AMOLED pixel circuit with a compensating scheme for variations in subthreshold slope and threshold voltage of driving TFTs. *IEEE J. Sol. State Circ.* **55**, 3087–3096 (2020).
- Takechi, K., Nakata, M., Eguchi, T., Yamaguchi, H. & Kaneko, S. Temperature-dependent transfer characteristics of amorphous InGaZnO4 thin-film transistors. *Jpn. J. Appl. Phys.* **48**, 011031-1–011301-6 (2009).
- Estrada, M. et al. Temperature dependence of the electrical characteristics of low-temperature processed zinc oxide thin film transistors. *Thin Sol. Films* **573**, 18–21 (2014).
- Abe, K. et al. Mobility- and temperature-dependent device model for amorphous In–Ga–Zn–O thin-film transistors. *Thin Sol. Films* **559**, 40–43 (2014).
- Jeong, J., Jeong, J. K., Park, J. S., Mo, Y. G. & Hong, Y. Meyer–Neldel rule and extraction of density of states in amorphous indium–gallium–zinc–oxide thin-film transistor by considering surface band bending. *Jpn. J. Appl. Phys.* **49**, 03CB02-1–03CB02-6 (2010).
- Chen, S., Abe, K., Kumomi, H. & Kanicki, J. Density of states of a-InGaZnO from temperature-dependent field-effect studies. *IEEE Trans. Electron. Dev.* **56**, 1177–1183 (2009).
- Li, J. et al. Temperature stress on a thin film transistor with a novel BaZnSnO semiconductor using a solution process. *RSC Adv.* **5**, 9621–9626 (2015).
- Zhou, Y. H., Li, J., Zhong, D. Y., Li, X. F. & Zhang, J. H. Enhanced stability of Sr-doped aqueous In₂O₃ thin-film transistors under bias/illumination/thermal stress. *IEEE Trans. Electron. Dev.* **66**, 1308–1313 (2019).
- Jeon, J. K., Um, J. G., Lee, S. & Jang, J. Control of O–H bonds at a-IGZO/SiO₂ interface by long time thermal annealing for highly stable oxide TFT. *AIP ADVANCES* **7**, 125110-1–125110-7 (2017).
- Yoon, S. H., Cho, J. H., Cho, I., Kim, M. J., Hur, J. S., Bang, S. W., Lee, H., Bae, J. U., Kim, J., Shong, B. & Jeong, J. K. Tailoring subthreshold swing in A-IGZO thin-film transistors for amoled displays: Impact of conversion mechanism on peald deposition sequences. *Small Methods* **8**, 2301185-1–2301185-12 (2024).
- Khan, K., Islam, M. E. & Akbar, M. A. Bifurcation, stability, and nonlinear parametric effects on the solitary wave profile of the Riemann wave equation. *Int. J. Theor. Phys.* **63**, 150 (2024).
- Islam, S. M. R., Islam, M. E., Akbar, M. A. & Kumar, D. The stretch coordinate effect, bifurcation, and stability analysis of the nonlinear Hamiltonian amplitude equation. *Partial. Differ. Equ. Appl. Math.* **13**, 101126 (2025).
- Hong, S. Y. et al. Study on the lateral carrier diffusion and source-drain series resistance in self-aligned top-gate coplanar InGaZnO thin-film transistors. *Sci. Rep.* **9**, 1–11 (2019).
- Na, J. et al. Interfacial thermal resistance effect in self-aligned top-gate a-IGZO thin film transistors. *Curr. Appl. Phys.* **65**, 91–95 (2024).
- Han, W. H. & Chang, K. J. Subgap states near the conduction-band edge due to undercoordinated cations in amorphous In–Ga–Zn–O and Zn–Sn–O semiconductors. *Phys. Rev. Appl.* **6**, 044011 (2016).
- Jana, K., Liu, S., Toprasertpong, K., Jiang, Q., Wahid, S., Kang, J., Chen, J., Pop, E. & Wong, H. S. P. Modeling and understanding threshold voltage and subthreshold swing in ultrathin channel oxide semiconductor transistors. *2024 SISPAD*, 01–04 (2024).
- Tsuji, H., Kamakura, Y. & Taniguchi, K. Drain current model for thin film transistors with interface trap states. *J. Appl. Phys.* **107**, 034502-1–034502-5 (2010).
- Guo, J. et al. Analytical surface potential-based compact model for independent dual gate a-IGZO TFT. *IEEE Trans. Electron. Dev.* **68**, 2049–2055 (2021).
- Lee, S. & Nathan, A. Localized tail state distribution in amorphous oxide transistors deduced from low temperature measurements. *Appl. Phys. Lett.* **101**, 113502-1–113502-5 (2012).
- Lee, S., Jeon, S. & Nathan, A. Modeling sub-threshold current–voltage characteristics in thin film transistors. *J. Display Technol.* **9**, 883–889 (2013).
- He, H. et al. Analytical drain current and capacitance model for amorphous InGaZnO TFTs considering temperature characteristics. *IEEE Trans. Electron. Dev.* **67**, 3637–3644 (2020).
- Bae, M. et al. Analytical current and capacitance models for amorphous indium–gallium–zinc–oxide thin-film transistors. *IEEE Trans. Electron. Dev.* **67**, 3637–3644 (2020).
- Cheng, X., Lee, S., Yao, G. & Nathan, A. TFT compact modeling. *J. Display Technol.* **12**, 898–906 (2016).
- Iniguez, B., Picos, R., Estrada, M., Cerdeira, A., Ytterdal, T. A., Jackson, W., Koudymov, A., Veksler, D. & Shur, M. S. Modelling of thin film transistors for circuit simulation. in *14th International Conference on Mixed Design of Integrated Circuits and Systems* 35–40 (2007).
- Chen, H. C. et al. Hydrogen diffusion and threshold voltage shifts in top-gate amorphous InGaZnO thin-film transistors. *IEEE Trans. Electron. Dev.* **67**, 3123–3128 (2020).
- Kang, D. H., Han, J. U., Mativenga, M., Ha, S. H. & Jang, J. Threshold voltage dependence on channel length in amorphous-indium–gallium–zinc–oxide thin-film transistors. *Appl. Phys. Lett.* **102**, 083508 (2013).
- Hu, G. J., Chang, C. & Chia, Y. T. Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's. *IEEE Trans. Electron. Dev.* **12**, 2469–2475 (1987).
- Bae, H., Jun, S., Jo, C. H., Choi, H., Lee, J., Kim, Y. H., Hwang, S., Jeong, H. K., Hur, I., Kim, W., Yun, D., Hong, E., Seo, h., Kim, D. H. & Kim, D. M. Modified conductance method for extraction of subgap density of states in a-IGZO thin-film transistors. *IEEE Electron. Dev. Lett.* **33**, 1138–1140 (2012).
- George, W. M., Kyle, T. V., John, F. W. & Matt, W. G. Illuminating trap density trends in amorphous oxide semiconductors with ultrabroadband photoconduction. *Adv. Funct. Mater.* **33**, 2300742-1–2300742-10 (2023).
- Kim, Y. M., Park, J. K., Ko, W. S., Kim, K. N. & Lee, G. W. Characterization of ZnO thin-film transistors with various active layer structures after exposure to different proton energies. *J. Semicond. Technol. Sci.* **24**, 63–68 (2024).
- Saito, N., Sawabe, T., Kataoka, J., Ueda, T., Tezuka, T. & Ikeda, K. High mobility (>30 cm² V^{−1} s^{−1}) and low source/drain parasitic resistance In–Zn–O BEOL transistor with ultralow <10–20 A μm^{−1} off-state leakage current. *Jpn. J. Appl. Phys.* **58**, SBBJ07-1–SBBJ07-7 (2019).

Acknowledgements

This research was supported by Samsung Display Co., Ltd., Chung-Ang University Research Scholarship Grants in 2024, and National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT)

(RS-2023-NR076667).

Author contributions

C.E.O. and H.S.J. developed the compact model. C.E.O., H.S.J., S.H.L. and H.W.L. performed numerical calculations and analyzed the results. D.H.S. and C.H.K. measured the electrical characteristics of the devices and conducted the analysis. M.H.K., K.S.S., and J.H.L. fabricated the devices. C.E.O., H.S.J., and H.I.K. wrote the manuscript. The project was supervised by S.S.H. and H.I.K.

Declarations

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to S.-H.S. or H.-I.K.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by/4.0/>.

© The Author(s) 2025