

LETTER OPEN ACCESS

Background Injection-Pulse Duty Correction With 0.05% Accuracy for Dual-Edge ILPLL Using Sub-Sampling Charge Pump

Dong-Hyun Yoon^{1,2}  | Tony Tae-Hyoung Kim² | Kwang-Hyun Baek³

¹Memory Division, Samsung Electronics, Hwaseong, South Korea | ²Centre for Integrated Circuits and Systems, Nanyang Technological University, Singapore |

³School of Electrical and Electronics Engineering, Chung-Ang University, Seoul, South Korea

Correspondence: Kwang-Hyun Baek (kbaek@cau.ac.kr)

Received: 4 June 2025 | **Revised:** 31 August 2025 | **Accepted:** 8 September 2025

Funding: This research was supported by the Chung-Ang University Research Grants in 2023.

ABSTRACT

This paper proposes a background duty-cycle corrections (DCC) scheme for a dual-edge injection locking phase-locked loop. Dual-edge injection enhances noise performance by effectively doubling the injection ratio. However, noise and spurs are highly sensitive to the duty cycle distortion. The proposed DCC scheme senses the duty-cycle conventional duty correction technique directly senses the duty of the injection pulse. The proposed DCC scheme is implemented in a 65 nm CMOS process and achieves a duty error correction accuracy of 0.05% under 3-sigma mismatch conditions.

1 | Introduction

Injection-locked phase-locked loops (ILPLLs) have been widely employed in system-on-chips (SoCs), such as microprocessors and wireless radio systems, due to their low phase noise and area efficiency [1]. Although ring oscillators (ROs) typically exhibit worse phase noise compared to LC oscillators, ILPLLs [2–4] achieve low noise by periodically initializing the accumulated jitter of the RO using the reference clock. The output noise is determined by the injection ratio, defined as the frequency ratio between the oscillator output and the reference clock. Dual-edge injection increases this ratio by generating injection pulses on both the rising and falling edges of the reference clock.

However, duty-cycle distortion in the reference clock severely degrades the performance of ILPLLs [2], making duty-cycle correction (DCC) essential. Figure 1a illustrates conventional DCC architecture. In ILPLLs, short injection pulses are generated to initialize the oscillator's jitter. Conventionally, the duty cycle

is sensed by extracting the DC component of the clock and comparing it with a reference voltage [5–7]. However, this method fails to detect distortions introduced by the pulse generator itself. This limitation becomes particularly significant in dual-edge injection schemes, where XOR gates are typically used, and designing symmetric XOR gate is challenging.

To overcome this limitation, the proposed DCC directly senses the duty of the injection pulses, as illustrated in Figure 1b. In this work, a sub-sampling phase detector [3] is adopted to measure the duty of extremely narrow injection pulses with high accuracy.

2 | Proposed Duty Correction Scheme

Figure 2 shows the architecture of the proposed ILPLL incorporating DCC. Since the phase difference between the injection pulse and the PLL is critical in ILPLLs, sub-sampling delay-locked loop (SS-DLL) is adopted for phase alignment [3]. SS-DLL consists of a sub-sampling phase detector (SSPD), charge pump (SSCP),

This is an open access article under the terms of the [Creative Commons Attribution](https://creativecommons.org/licenses/by/4.0/) License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

© 2025 The Author(s). *Electronics Letters* published by John Wiley & Sons Ltd on behalf of The Institution of Engineering and Technology.

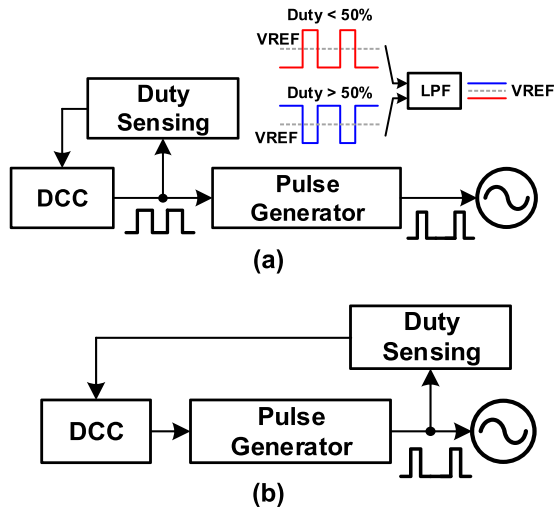


FIGURE 1 | Block diagram of (a) conventional and (b) proposed injection locking PLL with DCC.

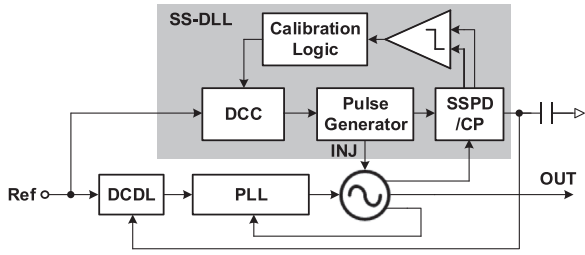


FIGURE 2 | Block diagram of Injection-locking PLL with proposed duty correction scheme.

and digitally controlled delay line (DCDL). The SSPD samples the VCO output using the injection pulses, after which the SSCP generates an analogue voltage fed into the VDL. As a result, VCO output is aligned with the injection pulse.

Figure 3a shows the schematic of the sub-sampling phase charge pump (SSCP) and the comparator, while Figure 3b illustrates the corresponding timing diagram. The SSCP consists of a pre-amplifier, which amplifies the sampled signals V_{SP} and V_{SN} , and a SSCP converts these signals into output currents. The comparator, which determines the duty of the injection pulses, shares the output of the pre-amplifier.

The signals V_{SP} and V_{SN} are sampled voltage of the VCO output captured by the injection pulses. When the injection pulse is low, these sampled values are held constant. Based on the amplitude difference between V_{SP} and V_{SN} , the phase lead or lag between the VCO and injection pulses is determined. When the CK_{SS} is activated, the SSCP adjusts the VDL according to V_{SP} and V_{SN} . As a result, the rising edge of the injection pulse aligns with the VCO output.

Figure 3b illustrates the SSCP output under two conditions: when the duty cycle is below and above 50%. Even if the SS-DLL aligns the rising-edge injection pulse with the VCO output, the injection pulses are still generated on both edges of the reference clock. As a result, duty-cycle asymmetry distorts the output signal. The

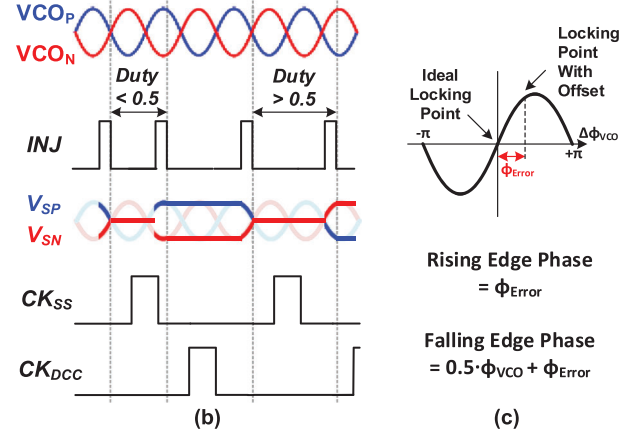
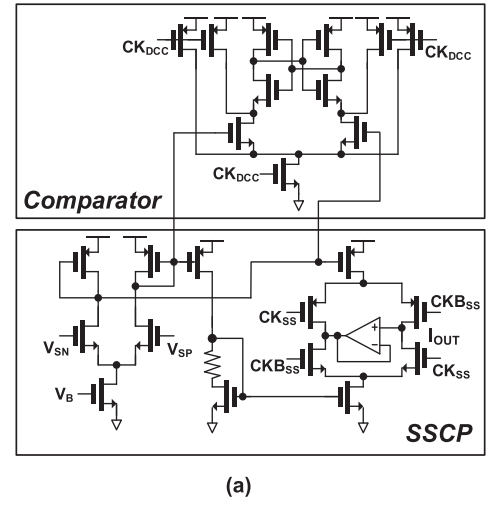


FIGURE 3 | (a) Schematic and (b) timing diagram of sub-sampling charge pump with comparator, and (c) phase offset due to offset.

power of m th harmonic with duty-cycle error is expressed as follows [2]:

$$P_m = \left(\left(\frac{2A}{m\omega_{REF}T_R} \cos(m\omega_{REF}2(t_{out2} - NT_R)/4) \cdot \sec(m\omega_{REF}T_R/4) \cdot \sin(mN\omega_{REF}T_R/4) \right) \right)^2 \quad (1)$$

where, A is the amplitude of reference clock and t_{out2} is the output time shift due to duty-cycle distortion. Then, the output spur on $m \cdot f_{REF}$ is given by

$$\text{spur} = 10 \cdot \log_{10} (P_m / P_{\text{Signal}}) \quad (2)$$

where P_{Signal} is signal power at fundamental frequency. In the proposed architecture, since the rising edge is already aligned by the DLL, the falling-edge pulse is used to extract duty-cycle information. As shown in Figure 3b, when $V_{SP} > V_{SN}$, the duty cycle is less than 50%. Conversely, when $V_{SP} < V_{SN}$, the duty exceeds 50%. The comparator outputs the duty information when the duty control clock CK_{DCC} is high. Since CK_{SS} and CK_{DCC} are alternately enabled, the proposed system simultaneously supports DLL and DCC operations, facilitating background duty-cycle calibration.

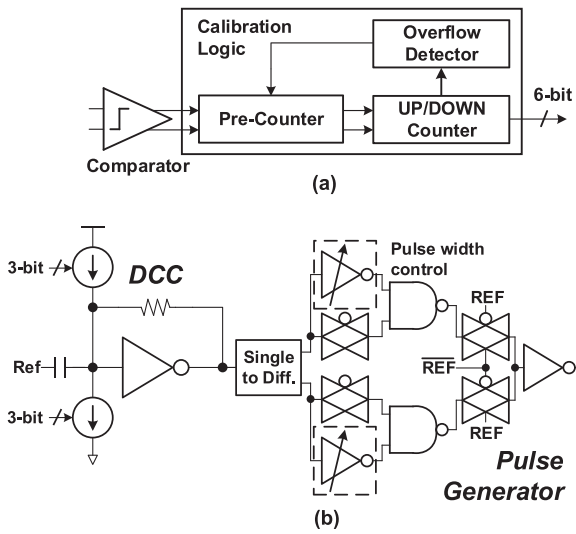


FIGURE 4 | (a) Block diagram of duty calibration logic and (b) schematic of 6-bit duty-cycle correction circuit and injection pulse generator.

The mismatches of the SSCP cause a phase error (Φ_{Error}), as shown in Figure 3c. However, the phase offset resulting from the mismatch occurs equally in both the rising-edge and falling-edge injection pulses. Therefore, the error between the two pulses is fixed at half of the VCO phase ($0.5 \cdot \Phi_{\text{VCO}}$), and the SSCP offset does not affect the operation of the DCC.

Figure 4a shows the block diagram of the calibration logic. The comparator output is fed into a pre-counter that adjusts the DCC loop gain. The signal is then converted into a 6-bit digital code by an up/down counter and sent to the DCC circuit shown in Figure 4b. The DCC circuit is implemented using an inverter with ac-coupling capacitors and resistive feedback. A 6-bit DAC connected to the AC-coupling node sets the common-mode voltage, enabling duty-cycle adjustment. The designed DCC covers a duty range from 48.5% to 51.5%. Figure 4b also depicts the proposed MUX-based dual-edge pulse generator. Unlike conventional XOR-based generators, which suffer from poor input symmetry, the proposed design employs NAND gates and a MUX to improve edge balance. The pulse width control block is also integrated to adjust the injection pulse width.

3 | Implementation and Simulation Results

The ILPLL with the proposed duty correction scheme is implemented with 65 nm CMOS process. Figure 5 shows the layout of the prototype of ILPLL without loop filter. A 100 MHz reference clock is used, and a 3.2 GHz output is generated by the prototype ILPLL.

Figure 6a shows the results of 1000-point Monte Carlo simulations for the duty cycles of the DCC output and injection pulse. Despite employing the symmetric pulse generator shown in Figure 4b, the injection pulse generator exhibits an average duty offset of -0.2% , with maximum and minimum offsets of $+2.5\%$ and -1.1% , respectively. Additional mismatches from logic gates introduce a 3σ variation of 2.1% . Therefore, the offset of

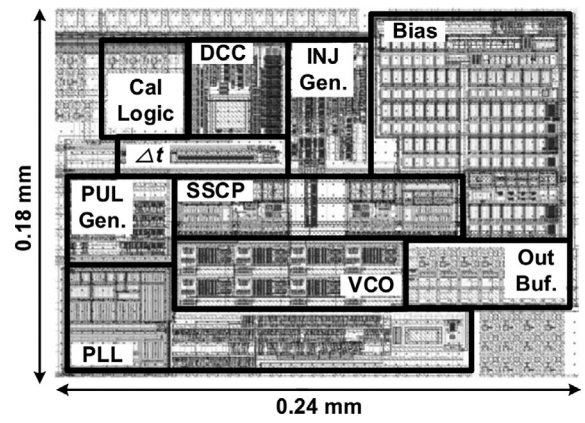


FIGURE 5 | Layout of ILPLL with proposed duty correction circuit.

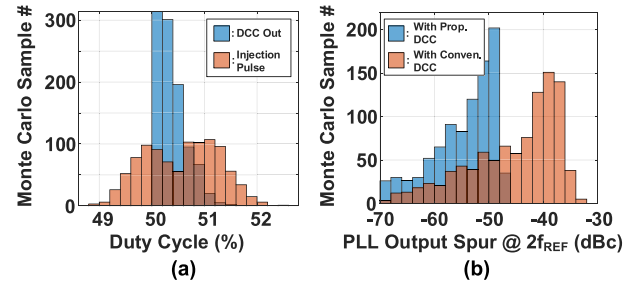


FIGURE 6 | Monte Carlo simulation results of (a) DCC/pulse generator output and (b) PLL output spur at $2f_{\text{REF}}$ frequency.

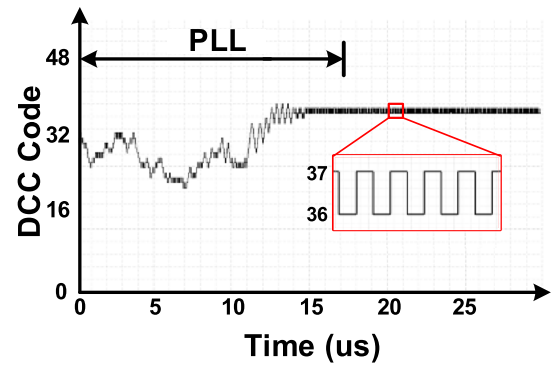


FIGURE 7 | Transient simulation result of proposed duty correction scheme.

pulse generator should be calibrated. Since the proposed DCC directly detects the duty cycle distortion of injection pulse, it effectively compensates for both static offset and random mismatch. Figure 6b shows PLL output spur at the $2f_{\text{REF}}$ frequency, where the worst-case spur is improved by 15.7 dB, from -32 to -47.7 dBc.

Figure 7 presents the transient response. Before $15 \mu\text{s}$, the PLL is in its settling phase. To ensure loop stability, the pre-counter in Figure 4a adjusts the DCC loop gain during this period. After locking, the DCC converges rapidly.

Table 1 shows the performance comparison of recent DCC. The total power consumption of the prototype PLL is 9.9 mW, of which

TABLE 1 | Performance comparison table.

	This work^a	[5]	[6]	[7]
Process (nm)	65	55	40	55
Frequency (GHz)	0.1	1-5	4-8	32
Power (mW)	0.5	3.6	4.7	0.03
Duty range (%)	48.5–51.5	20–80	—	20–80
Duty accuracy (%)	0.05	0.1	0.8	0.5
Sensing point	Injection short pulse	Common clock	Common clock	Common clock
Area (mm ²)	0.0072	0.0017	0.0082	0.0064

^aSimulation result.

the proposed DCC, including its sensing and correction circuits, accounts for only 0.5 mW, introducing minimal overhead. With a resolution of 0.05%, the duty distortion remains below 0.05% after correction. This paper is the first to sense duty-cycle distortion of the short pulse used in an injection-locked PLL.

4 | Conclusion

A duty-cycle correction scheme is proposed for ILPLLs to directly sense and compensate distortion in narrow injection pulses. Conventional architecture cannot correct the offset and mismatch originating from the pulse generator. In contrast, the proposed scheme directly senses the injection pulse, enabling compensation of both offset and mismatch. Consequently, the maximum offset of 2.5% and a 3σ mismatch of 2.1% were eliminated, achieving duty-cycle correction with 0.05% accuracy.

Author Contributions

Dong-Hyun Yoon: conceptualization, investigation, writing – original draft preparation. **Tony Tae-Hyoung Kim:** supervision, writing – review & editing. **Kwang-Hyun Baek:** project administration, supervision, writing – review & editing.

Acknowledgements

This research was supported by the Chung-Ang University Research Grants in 2023.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

1. J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S.-J. Kim, and P. K. Hanumolu, “19.8 A 0.0021mm² 1.82 mW 2.2 GHz PLL Using Time-Based Integral Control in 65Nm CMOS,” in 2016 IEEE International Solid-State Circuits Conference (ISSCC) (IEEE, 2016), 338–340.
2. S.-Y. Cho, S. Kim, M.-S. Choo, et al., “A 2.5–5.6 GHz Subharmonically Injection-Locked All-Digital PLL With Dual-Edge Complementary Switched Injection,” *IEEE Transactions on Circuits and Systems I: Regular Papers* 65, no. 9 (September 2018): 2691–2702, <https://doi.org/10.1109/TCSI.2018.2799195>.
3. D.-H. Yoon, D.-K. Jung, K. Seong, et al., “A 3.2-GHz 178-fsrms Jitter Subsampling PLL/DLL-Based Injection-Locked Clock Multiplier,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 30, no. 7 (July 2022): 915–925, <https://doi.org/10.1109/TVLSI.2022.3169636>.
4. Z. Wang, X. Zheng, Y. He, et al., “A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Injection-Locked Clock Multiplier Utilizing a Complementary-Injection Scheme and an Adaptive Pulsewidth Adjustment,” *IEEE Journal of Solid-State Circuits* 60, no. 3 (March 2025): 799–812, <https://doi.org/10.1109/JSSC.2024.3486291>.
5. Y. Qiu, Y. Zeng, and F. Zhang, “1–5 GHz Duty-Cycle Corrector Circuit With Wide Correction Range and High Precision,” *Electronics Letters* 50, no. 11 (May 2014): 792–794, <https://doi.org/10.1049/el.2014.0170>.
6. G. Park, J. Han, and W. Bae, “Design and Analysis of Asynchronous Sampling Duty Cycle Corrector,” *Electronics* 10, no. 21 (October 2021): 2594, <https://doi.org/10.3390/electronics10212594>.
7. D. G. Kim, J.-M. Yoo, Y. G. Pu, et al., “A Reference Clock Doubler With Fully Digital Duty-Cycle Error Correction Controller,” *Journal of Semiconductor Technology and Science* 21, no. 6 (December 2021): 1598–1657, <https://doi.org/10.5573/JSTS.2021.21.6.466>.