

Received 3 January 2026, accepted 5 February 2026, date of publication 11 February 2026, date of current version 19 February 2026.

Digital Object Identifier 10.1109/ACCESS.2026.3663750

RESEARCH ARTICLE

A 2.4-GHz Type-I Reference-Sampling Injection-Locked PLL With an RSPD-Based Injection Timing Calibration Loop

JOOHEE LEE^{1,2}, (Member, IEEE), JAE-SOUB HAN^{1,2}, (Member, IEEE),
JONGHYUN SEO², (Member, IEEE), DONG-HYUN YOON^{3,4}, (Member, IEEE), AND
KWANG-HYUN BAEK^{1,4}, (Senior Member, IEEE)

¹Mobile Division, Dongwon Anatech, Seoul 06716, South Korea

²Department of Intelligent Semiconductor Engineering, Chung-Ang University, Seoul 06974, South Korea

³Memory Division, Samsung Electronics, Hwaseong-si 18448, South Korea

⁴School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 06974, South Korea

Corresponding author: Dong-Hyun Yoon (kindyoon27@naver.com)

This work was supported in part by Korea Planning and Evaluation Institute of Industrial Technology (KEIT) funded by the Ministry of Trade, Industry and Energy (MOTIE), South Korea, under Grant RS-2025-02413438.

ABSTRACT A type-I reference-sampling injection-locked phase-locked loop (RS-ILPLL) for low-jitter clock generation is presented. For the first time, the proposed architecture integrates a reference-sampling PLL (RSPLL) with an injection-locked PLL (IL-PLL), combining the wide lock range and inherent stability of the RSPLL with the noise-suppression capability of injection locking. An RSPD-based injection timing calibration loop is also introduced to precisely align the phase between the PLL and injection paths by compensating intrinsic delay mismatches. Fabricated in a 65-nm CMOS process, the prototype occupies a core area of 0.24 mm² and consumes 5.78 mW at 2.4-GHz. The RS-ILPLL achieves a 9.1 dB phase-noise improvement and an integrated RMS jitter of 92.6 fs ($FoM_1 = -253$ dB, $FoM_2 = -266.8$ dB), corresponding to a 72 % reduction compared with a conventional type-I RSPLL. Owing to its stable loop dynamics and compact implementation, the proposed RS-ILPLL demonstrates fast locking, low power, and robust low noise performance without requiring an auxiliary FLL. These features make it highly suitable for next-generation high-speed clocking applications.

INDEX TERMS Reference-sampling PLL (RSPLL), injection-locked clock multiplier (ILCM), injection-locked PLL (IL-PLL), low jitter, self-aligned injection timing.

I. INTRODUCTION

Low-power and low-jitter phase-locked loops (PLLs) are essential building blocks in modern high-speed systems. In many emerging applications, such as high-speed wireline transceivers, wireless communication systems, and high-resolution data converters, the quality of the clock directly determines overall system performance. Therefore, achieving robust and low-jitter clock generation is a key design requirement for mixed-signal platforms. Among various PLL architectures, the injection-locked clock multiplier (ILCM)

[1], [2], [3], [4], [5], [6] has attracted significant attention due to its simple architecture and ultra-low-jitter characteristics.

However, maintaining the ultra-low-jitter performance of ILCMs requires frequency calibration loop to compensate for frequency drift caused by process, voltage, and temperature (PVT) variations. The most widely used approach is frequency-locked loop (FLL)-based calibration [7], [8], [9], which provides effective initial frequency alignment. Nevertheless, as illustrated in Fig. 1, since FLLs are disabled after initial frequency locking, they cannot continuously compensate for frequency drift caused by temperature variation and aging effects, which may result in excessive reference spurs or even lock failures. In contrast, PLL-based

The associate editor coordinating the review of this manuscript and approving it for publication was Mohammad Hossein Moaiyeri¹.

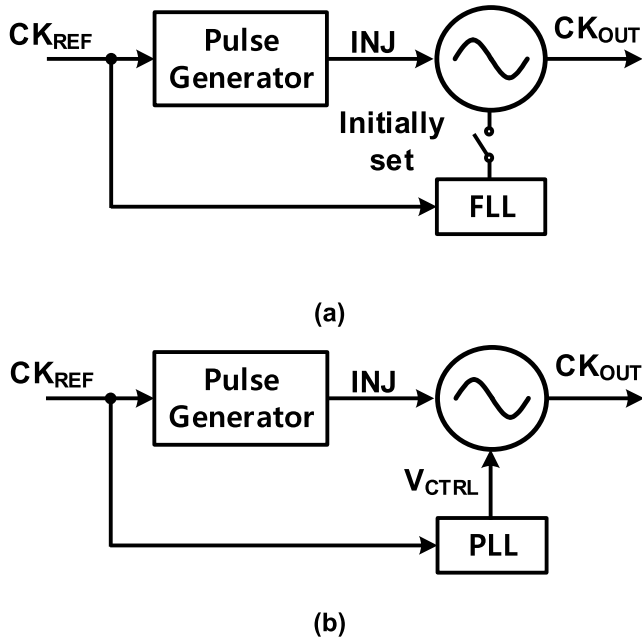


FIGURE 1. Block diagram of ILPLL with (a) FLL-based and (b) PLL-based calibration.

calibration [10], [11], [12], [13] can continuously adjust the VCO control voltage (V_{CTRL}) through loop feedback, thereby offering stronger robustness against PVT variations. Despite these advantages, achieving both continuous frequency calibration and low-jitter performance remains challenging, as additional calibration loops introduce extra in-band noise and design complexity.

A. LIMITATIONS OF CONVENTIONAL SAMPLING-BASED ILCMS

Conventional PLL-based ILCMs (IL-PLL) achieve low-noise performance by suppressing VCO phase noise through injection. However, they remain limited by the in-band noise contributions of the phase-frequency detector (PFD), charge pump (CP), and divider. Consequently, sampling-based IL-PLLs have emerged as an attractive alternative, since they can mitigate not only VCO noise but also in-band noise within the loop bandwidth (f_{BW}), thereby further improving overall noise performance.

As mentioned above, sampling-based PLLs are a promising technique for achieving low in-band noise performance. Fig. 2 compares the phase detector (PD) characteristics of two representative sampling-based PLLs: the sub-sampling PLL (SSPLL) [14], [15] and the reference-sampling PLL (RSPLL) [15], [17]. Because the SSPLL samples the VCO output using the reference clock, it exhibits a narrow lock range and an excessively high PD gain. As a result, an auxiliary FLL is typically required to guarantee initial locking. Furthermore, the high PD gain causes small phase errors to translate into large sampling voltage errors, thereby demanding a large loop filter area to ensure loop stability. In contrast, RSPLL samples the reference clock using the VCO output. Thus,

RSPLLs inherently provide a wide lock range, enabling stable operation without auxiliary loops and allowing for compact loop-filter implementations.

Fig. 3 illustrates a conceptual phase-noise comparison among a conventional IL-PLL and a sampling-based IL-PLL. In conventional IL-PLLs, the in-band noise contributed by the PFD/CP and the divider scales with the square of the division ratio N^2 , while the noise reduction effect of injection diminishes at low frequencies [18]. In contrast, a sampling-based IL-PLL replaces the PFD/CP and divider with a sampling-based phase detector, thereby eliminating the N^2 -scaled in-band noise, similar to conventional sampling-based PLLs [14], [15], [17].

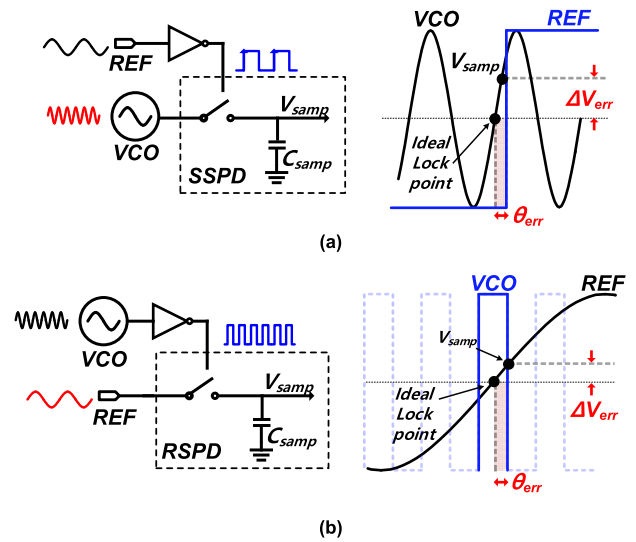


FIGURE 2. Characteristics of (a) SSPLL and (b) RSPLL.

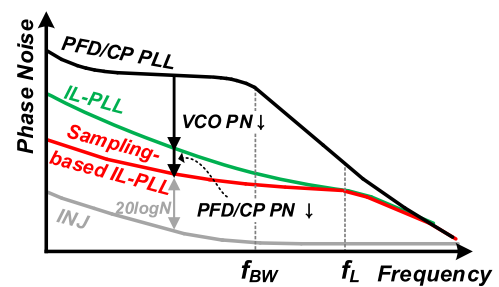


FIGURE 3. Conceptual phase-noise comparison among PFD/CP PLL, IL-PLL, and sampling-based IL-PLL architectures.

To address these limitations, sub-sampling-based IL-PLLs (SS-ILPLL) [18], [19], [20], [21] have been reported, combining the injection mechanism with a sub-sampling phase detector. SS-ILPLLs eliminate the divider and thereby significantly reduce in-band noise. Despite the improved noise performance, they suffer from intrinsic limitations. The narrow lock range of the sub-sampling detector requires auxiliary FLLs for initial locking, and the high detector gain leads to large sampling voltage errors, demanding large loop

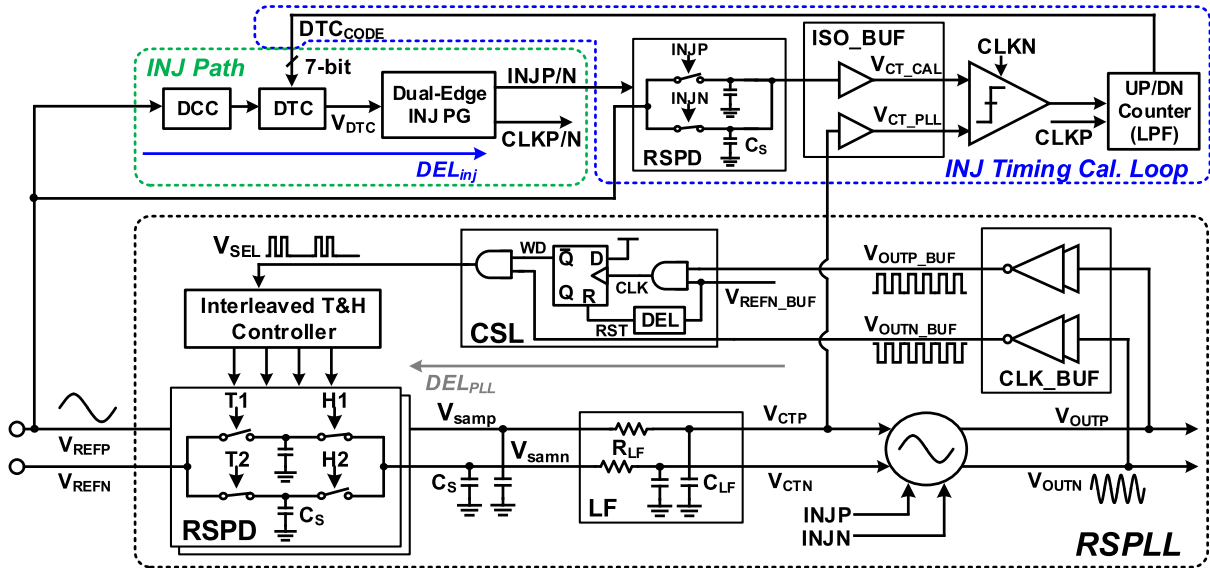


FIGURE 4. Proposed RS-ILPLL architecture with RSPD-based injection timing calibration loop.

filters for stabilization. As a result, their practical efficiency in terms of area and power remains limited.

RSPLL achieves low in-band noise performance by reducing the noise sources within the loop [17]. Furthermore, a type-I RSPLL can be adopted to further enhance the loop stability. A conventional type-I RSPLL exhibits a high phase margin and fast settling behavior owing to the single integrator in the loop (the VCO). However, because the loop has only one integrating pole, the VCO noise is filtered with only a -20 dB/dec roll-off slope, making it dominant in the in-band region. To address this limitation, [22] introduced a type-II RSPLL, in which an additional CP integrator forms a second pole, enabling -40 dB/dec slope filtering for enhanced low-frequency noise suppression. However, the added CP also introduces extra noise because the RSPD exhibits a lower gain than the sub-sampling PD, so a gain-boosting technique was employed to mitigate this CP-induced noise.

B. RS-ILPLL AND CONTRIBUTIONS

To overcome these challenges, this work proposes a reference-sampling injection-locked PLL (RS-ILPLL). The proposed architecture leverages the injection-locking mechanism to achieve additional VCO noise suppression even with a type-I loop configuration. This approach maximizes noise-reduction efficiency while maintaining a compact design, high loop stability, and fast locking characteristics inherent to the type-I structure. In addition to frequency calibration, a reference-sampling-based self-calibration loop is incorporated to precisely align the timing between the injection and PLL paths. Timing misalignment can degrade the injection effect, leading to residual spurs and jitter accumulation. The proposed loop continuously monitors and corrects this mismatch in the background, ensuring stable

locking behavior across PVT variations. Together, these techniques enable efficient timing calibration with minimal hardware overhead, while further enhancing robustness and power efficiency.

The main contributions of this work are summarized as follows: (1) A new RS-ILPLL architecture is presented that, for the first time, integrates a type-I RSPLL into an injection-locked clock multiplier, combining wide lock range and inherent loop stability with the noise suppression capability of injection locking. (2) An RSPD-based injection-timing calibration loop is proposed that directly senses the phase difference between the PLL and injection paths using sampled control voltages, enabling background timing alignment without additional analog phase detectors. (3) A 2.4-GHz prototype implemented in 65-nm CMOS demonstrates 92.6-fs integrated rms jitter, corresponding to a 72% reduction compared with a conventional type-I RSPLL, and achieves state-of-the-art jitter-power efficiency among PLL-based ILCMs.

This article is organized as follows. Section II describes the proposed architecture and detailed circuit implementations. Section III presents experimental results, and Section IV concludes the paper.

II. PROPOSED RS-ILPLL AND CIRCUIT DESIGN

Fig. 4 illustrates the overall architecture of the proposed reference-sampling injection-locked PLL (RS-ILPLL). The architecture consists of three main components: a type-I reference-sampling PLL (RSPLL), an injection path, and a reference-sampling-based injection timing calibration loop.

A. RS-ILPLL

The proposed RS-ILPLL employs a type-I reference-sampling PLL as the frequency calibrator. The RSPLL

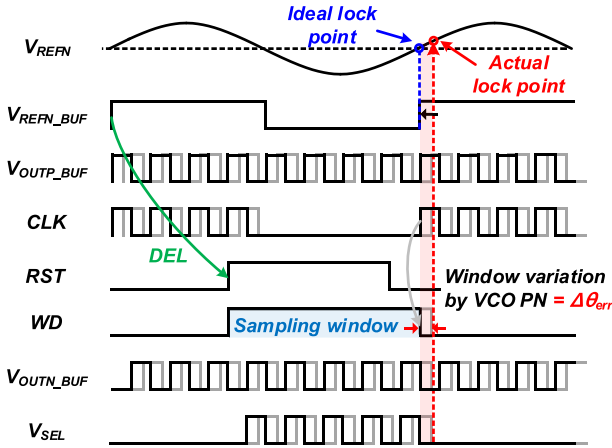


FIGURE 5. Timing diagram of clock selection logic.

consists of a VCO, a clock-selection logic (CSL), a time-interleaved track-and-hold (T&H) controller, an RSPD, and a loop filter. In this loop, the reference sine wave (V_{REFP} , V_{REFN}) is sampled by selected VCO pulses (V_{SEL}) through an RSPD, and the resulting sampled voltage (V_{smp} , V_{samm}) controls the VCO frequency. Fig. 5 illustrates the operation in which the clock-selection logic (CSL) extracts a subset of VCO pulses [23]. For optimal sampling, the reference signal is captured near its zero-crossing point, maximizing the RSPD gain and linearity. The sampling window is defined by two signals: its rising edge is triggered by the buffered reference signal (V_{REFN_BUF}), and its falling edge is derived from the buffered VCO output (V_{OUTP_BUF}). Within this window, the V_{OUTN_BUF} is gated to produce the final sampling pulse that captures the reference sine wave around the zero-crossing point. This approach enhances the RSPD noise performance and steers the oscillator frequency toward $N \cdot f_{REF}$ for rapid acquisition without an auxiliary FLL. In addition, the CSL reduces power consumption in the RSPD driver path, as only a subset of the VCO pulses is buffered. The time-interleaved ping-pong RSPD structure is implemented to mitigate sampling errors from charge injection and reference feedthrough caused by parasitic coupling. With a 3.7 pF sampling capacitor (C_s) and a 25 Ω switch on-resistance (R_{on}), the RSPD achieves an in-band noise level of -140.5 dBc/Hz (calculated) [23] and -143.2 dBc/Hz (simulated) at a 100 kHz offset, respectively.

However, because its first-order filtering characteristic provides only a -20 dB/dec attenuation slope, the type-I RSPLL cannot sufficiently suppress in-band VCO phase noise. As shown in Fig. 6, this VCO phase noise manifests as a residual phase error $\Delta\theta_{err}$, which leads to a sampling voltage error ΔV_{err} even after lock. In the CSL operation, as depicted in Fig. 5, this residual VCO phase noise causes timing variations of the V_{OUTP/N_BUF} , thereby modulating the width of the CSL window. Consequently, the varying window shifts the sampling point, producing ripples on V_{CT_PLL} . The injection technique mitigates this issue

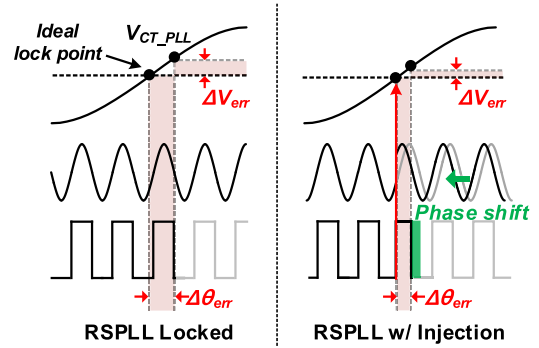


FIGURE 6. Phase error correction by injection after RSPLL locking.

effectively. Through the injection pulling/pushing mechanism, the VCO phase is realigned with reference, reducing the residual phase error. This phase correction suppresses the VCO-phase-noise-induced fluctuation of the CSL window and stabilizes the sampling instant.

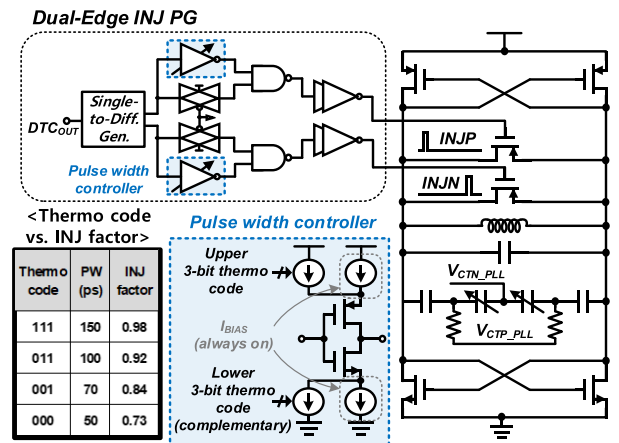


FIGURE 7. Dual-edge injection pulse generator with pulse width controller and digitally programmable injection strength, applied to a differential VCO.

To maximize the effectiveness of injection locking, both the injection strength and timing must be carefully optimized. The injection path consists of a 5-bit duty cycle corrector (DCC), a 7-bit digitally controlled digital-to-time converter (DTC), a dual-edge pulse generator (INJ PG). Dual-edge operation and a wide injection pulse width enhance the injection strength, thereby significantly improving noise suppression. As illustrated in Fig. 7, the INJP/N signals inject into the differential VCO on both the rising and falling edges of the reference clock, corresponding to a $2 \cdot f_{ref}$ injection rate that enables dual-edge operation. The injection pulse width is digitally adjustable through a 3-bit thermometer-coded current source, allowing the injection ratio to be tuned from 0.73 to 0.98. To ensure accurate dual-edge injection, the DCC compensates for reference clock duty errors, as shown in Fig. 8. The DCC supports up to $\pm 3.3\%$ correction with 0.1% LSB resolution. The DTC provides a 250 ps delay range

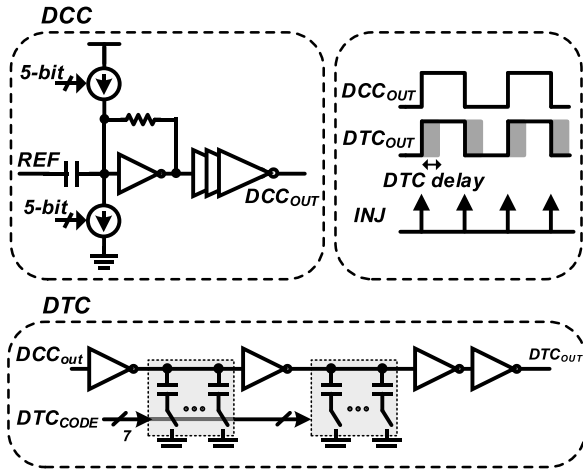


FIGURE 8. Duty cycle corrector and digital-to-time converter circuit.

with 2 ps resolution, offering sufficient margin beyond the 208 ps half-period of the VCO clock, thereby enabling fine alignment of the injection signal with the VCO zero crossing.

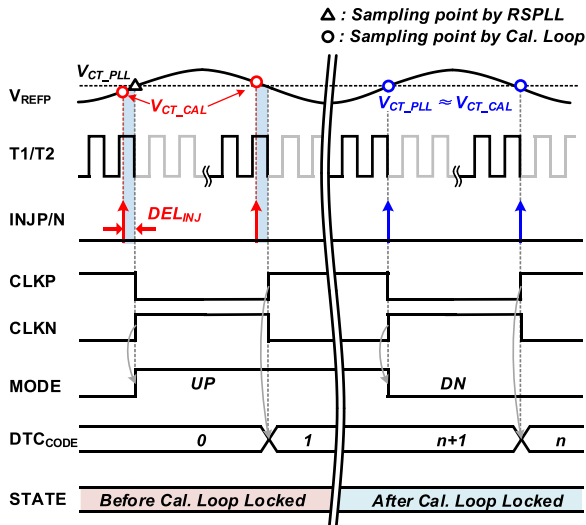


FIGURE 9. Timing diagram of RSPD-based injection calibration.

B. RSPD-BASED INJECTION TIMING CALIBRATION LOOP

This work proposes an RSPD-based injection timing calibration loop that utilizes the wide lock range of the RSPD. As shown in Fig. 4, the proposed calibration loop consists of an RSPD, an isolation buffer, a strong-arm latch comparator, and a 7-bit up/down counter. Accurate phase alignment between the injection and VCO signals is required to maximize noise suppression and ensure stable injection locking under PVT variations; therefore, the intrinsic delay of the injection path (DEL_{INJ}) must match the loop delay of the PLL (DEL_{PLL}).

Fig. 9 illustrates the operating principle of the injection timing calibration loop. To align the injection timing with

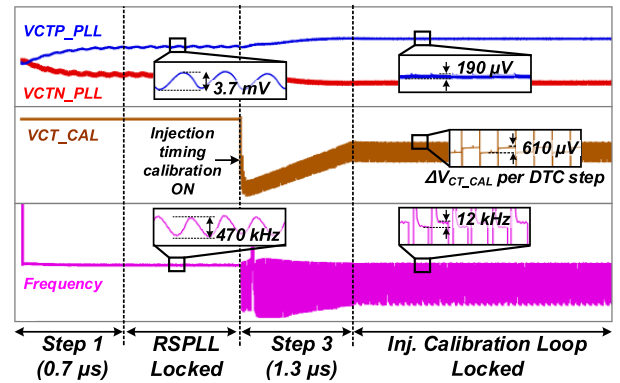


FIGURE 10. Transient simulation of the RS-ILPLL.

the VCO phase, this work exploits the fact that the sampled control voltages of the phase detector inherently contain phase error information. V_{CT_PLL} and V_{CT_CAL} correspond to the phase differences between the reference and each signal, and can be expressed as

$$V_{CT_PLL} = A \cdot (\sin(\theta_{REF}) - \sin(\theta_{VCO})) \quad (1)$$

$$V_{CT_CAL} = A \cdot (\sin(\theta_{REF}) - \sin(\theta_{INJ})), \quad (2)$$

where θ_{REF} , θ_{VCO} , θ_{INJ} , and A represent the phases of $V_{REFP/N}$, the VCO, and $INJ/P/N$, and the amplitude of $V_{REFP/N}$, respectively.

Their difference,

$$V_{CT_PLL} - V_{CT_CAL} = A \cdot (\sin(\theta_{INJ}) - \sin(\theta_{VCO})), \quad (3)$$

which means the relative phase offset between the VCO and injection paths. By minimizing this voltage difference, the proposed calibration loop aligns the injection phase with that of the VCO, achieving precise timing synchronization between DEL_{INJ} and DEL_{PLL} . The VCO and injection pulses sample the reference sine wave, generating V_{CT_PLL} and V_{CT_CAL} . The comparator compares these two control voltages. When $V_{CT_PLL} > V_{CT_CAL}$, the injection edge arrives earlier than the VCO edge (INJ leads), prompting an UP signal, which increases the DTC_{CODE} to add delay and thus slows the injection path. Conversely, when $V_{CT_PLL} < V_{CT_CAL}$ (INJ lags), a DN signal decreases DTC_{CODE} , reducing the delay and advancing the injection edge toward alignment.

The up/down counter functions as a low-pass filter and updates the 7-bit DTC_{CODE} according to the comparator's UP/DN signals. The updated code controls the DTC capacitor array to fine-tune the injection delay, aligning the injection edge with the VCO zero-crossing. When the calibration converges such that $V_{CT_PLL} \approx V_{CT_CAL}$, phase alignment between the injection and VCO pulses is achieved.

In the locked state, the DTC_{CODE} toggles between two adjacent values (n and $n+1$). The calibration loop can be disabled after locking to prevent undesired frequency modulation. This calibration effectively compensates for intrinsic phase misalignment in the injection path. A five-transistor OTA buffer is used as an isolation buffer to block

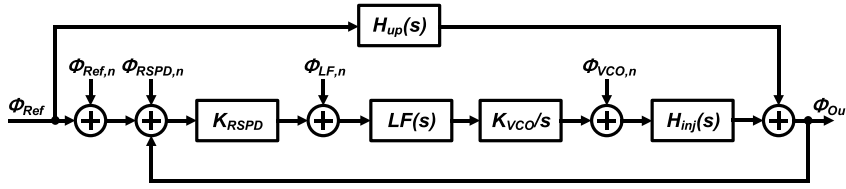


FIGURE 11. Phase domain model of the proposed RS-ILPLL.

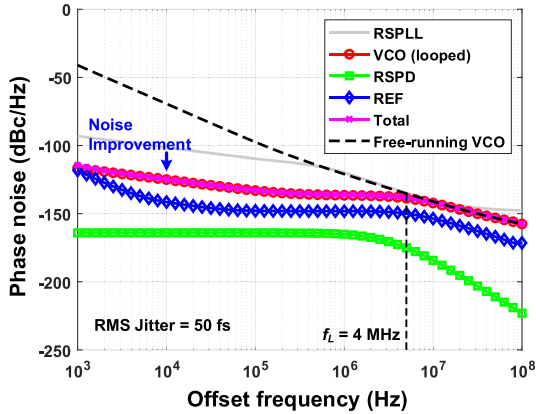


FIGURE 12. Simulated phase noise of the conventional type-I RSPLL and proposed RS-ILPLL.

kick-back noise from the comparator. This prevents voltage fluctuations and improves the RS-ILPLL noise performance.

Fig. 10 illustrates the locking behavior of the proposed RS-ILPLL. The operation consists of two main steps: Step 1, where the RSPLL locks to the reference, and Step 2, where the injection timing calibration loop is activated.

In Step 1, the RSPLL operates as a frequency calibrator and achieves fast locking within 0.7 μ s, owing to the inherent advantages of the type-I structure. After RSPLL locking, V_{CTP_PLL} still exhibits a peak-to-peak fluctuation of 3.7 mV caused by the steady-state phase error, which leads to a frequency deviation of 470 kHz that reflects the residual phase noise of the type-I RSPLL.

In Step 2, the injection and calibration loops are enabled. During this phase, V_{CTP_CAL} begins to track V_{CTP_PLL} , aligning the injection timing with the VCO phase. After the calibration loop locks, the DTC_{CODE} toggles between two adjacent values ($n, n+1$). A one-LSB difference of the DTC_{CODE} results in a voltage difference of about 610 μ V, introducing a small timing shift in the injection pulse. The calibration loop, also based on a type-I topology, settles within 1.3 μ s.

After both loops are locked, the ripple of V_{CTP_PLL} decreases from 3.7 mV to 190 μ V, and the VCO frequency deviation is reduced from 470 kHz to 12 kHz, confirming the effectiveness of the injection mechanism. The proposed RS-ILPLL achieves low-noise and stable operation with a wide lock range.

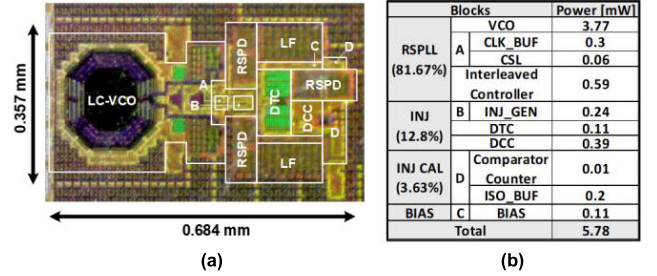


FIGURE 13. (a) Die photograph and (b) power breakdown.

C. PHASE DOMAIN ANALYSIS

Fig. 11 illustrates the phase domain model of the proposed architecture. The noise sources in the RS-ILPLL are suppressed by injection. The transfer functions for injection and reference up-conversion are defined in Equations (4) and (5) [24].

$$H_{inj}(j\omega) = 1 - \frac{\alpha e^{-j\omega T_{ref}} e^{-j\omega T_{ref}/2} \sin(\omega T_{ref}/2)}{1 + (\alpha - 1)e^{-j\omega T_{ref}}} \frac{\omega T_{ref}/2}{\omega T_{ref}/2} \quad (4)$$

$$H_{up}(j\omega) = 1 - \frac{N\alpha e^{-j\omega T_{ref}} e^{-j\omega T_{ref}/2} \sin(\omega T_{ref}/2)}{1 + (\alpha - 1)e^{-j\omega T_{ref}}} \frac{\omega T_{ref}/2}{\omega T_{ref}/2} \quad (5)$$

Fig. 12 shows the phase noise simulation results based on the phase domain model. In the conventional RS-PLL, the VCO noise is filtered with a slope of only -20 dB/dec. Therefore, despite the low noise levels of the reference and RSPD, it exhibits an integrated RMS jitter of 260 fs. In contrast, the proposed RS-ILPLL provides additional noise suppression below the locking frequency (f_L) owing to the injection locking. As a result, it achieves an integrated RMS jitter of 50 fs, representing an 81% reduction compared with that of the conventional design.

III. MEASUREMENT RESULTS

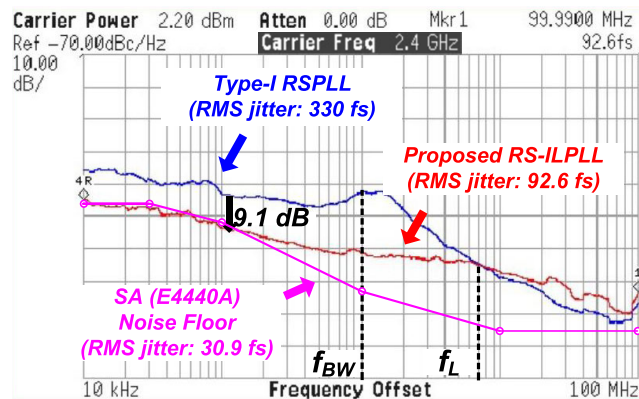
The proposed RS-ILPLL was fabricated in a 65-nm CMOS process and occupies a core area of 0.24 mm^2 , as shown in Fig. 13(a). The total power consumption is 5.78 mW from a 1.2 V supply. The detailed power distribution is summarized in Fig. 13(b). The RSPLL core accounts for 81.7 % of the total power, while the injection and calibration loops consume only 18.3 %, achieving superior noise suppression and timing calibration.

TABLE 1. Comparison with other ILCMs based on PLL.

	[6] JSCC'13	[20] TCAS-I'18	[19] ASSCC'19	[13] JSSC'20	[18] TVLSI'22	This work
Process [nm]	180	65	90	28	65	65
VCO Type	LC	Ring	LC	Ring	Ring	LC
Freq. Calibration	PFD/CP	SSBBPD	Sub-sampling	PFD/CP	Sub-sampling	Reference-sampling
Phase Calibration	BBPD	SSBBPD	SSPD	SSBBPD	Replica delay cell + SSPD	RSPD
Reference Freq. [MHz]	150	156.25	375	125	100	100
Output Freq. [GHz]	2.4	5	2.4	4	3.2	2.4
Integrated RMS Jitter [fs]	145 [10k-100M]	168 [1k-40M]	370 [10k-30M]	710 [10k-30M]	178 [10k-30M]	92.6 [10k-100M]
Spur ($f_{ref}/2f_{ref}$) [dBc]	-40	-42 / -42.6	-40	-61.6	-26.7 / -43.9	-43.9 / -25.1
Power [mW]	12.6	15.4	0.5	11.4	9.86	5.78
Area [mm ²]	0.64	0.06	0.26	0.09	0.87	0.24
* FOM ₁ [dB]	-246	-243.6	-251.6	-232.4	-245.1	-253
** FOM ₂ [dB]	-257.8	-258.7	-269.4	-247.5	-260.1	-266.8

$$*FOM_1 = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{dc}}{1mW}\right)\right]$$

$$*FOM_2 = 10\log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{dc}}{1mW}\right) \cdot \left(\frac{1}{N}\right)\right]$$

**FIGURE 14.** Measured phase noise of the conventional type-I RSPLL and the proposed RS-ILPLL.

A comparison of the measured phase noise between the conventional type-I RS-PLL and the proposed RS-ILPLL is shown in Fig. 14. The phase noise is measured using a spectrum analyzer (E4440A, Keysight). According to the datasheet [25], the noise floor of the spectrum analyzer is -116 dBc/Hz and -122 dBc/Hz at 10 kHz and 100 kHz offsets, respectively, and the integrated RMS jitter from 10 kHz to 40 MHz is 30.9 fs. Therefore, the measured low-frequency phase noise is limited by the spectrum analyzer's noise floor. The proposed design exhibits additional in-band VCO-noise suppression beyond the RSPLL f_{BW} (1 MHz), effectively extending the suppression range to f_L (4 MHz). At a 100-kHz offset, the proposed RS-ILPLL achieves a phase-noise improvement of 9.1 dB over the

conventional type-I RSPLL. The measured integrated RMS jitter is 92.6 fs, representing a 72% reduction from the 330 fs of the conventional type-I RSPLL. This improvement demonstrates the complementary effect of injection locking and reference-sampling calibration, which jointly suppress residual VCO phase noise and stabilize the sampling instant. Assuming uncorrelated jitter contributions, the de-embedded RMS jitter of the PLL is estimated to be approximately 87.3 fs after accounting for the instrument jitter of 30.9 fs.

Fig. 15(a) shows the measured spurs at -25.1 dBc ($2f_{ref}$) and -43.9 dBc (f_{ref}). The dominant $2f_{ref}$ spur mainly originated from the limitation of conventional injection switch. This spur can be mitigated by reducing the injection pulse width to minimize distortion introduced by injection switch. Furthermore, recent work in [26] reports that a conventional injection switch fundamentally limits the achievable reference spur to -31.8 dBc. By incorporating a recovery switch in the injection scheme, [26] demonstrates an improved spur level of -56.7 dBc. This indicates that the observed spur performance in this work is primarily constrained by the conventional injection architecture rather than by any structural limitation of the proposed PLL or calibration loop.

To verify process and supply robustness, Fig. 15(b) and (c) present the RMS jitter measured across ten samples and a wide supply voltage range. The maximum chip-to-chip jitter variation is below 28 fs, demonstrating stable operation and reliable convergence of the proposed calibration scheme. In addition, the proposed PLL exhibits a

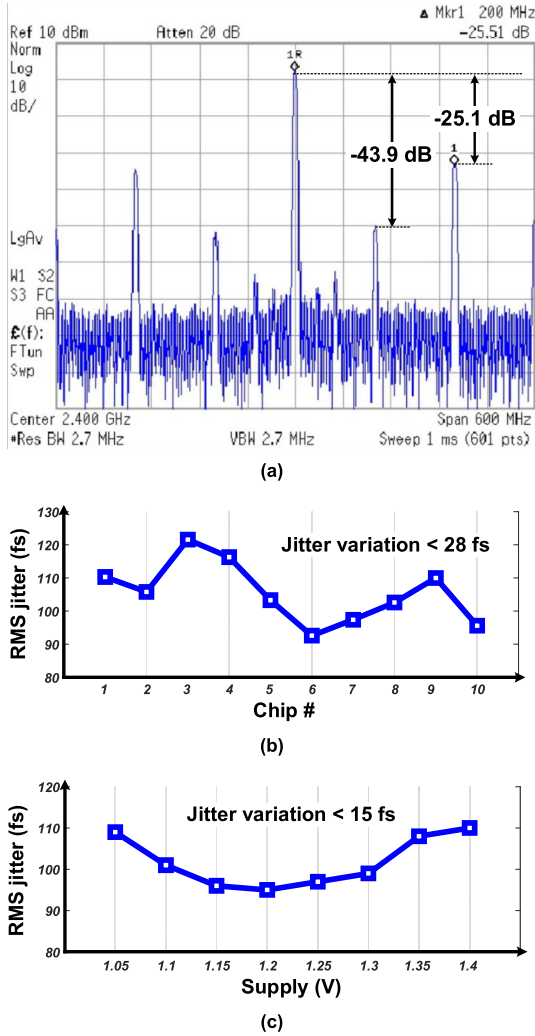


FIGURE 15. (a) Measured output spectrum and RMS jitter variation across (b) chips and (c) supply voltages.

jitter variation below 15 fs over a supply voltage from 1.05 V to 1.4 V.

Table 1 compares the proposed design with other ILCMs based on PLL architecture. This work is the first implementation that integrates a reference-sampling PLL (RSPLL) into an ILCM scheme, combining the wide lock range and inherent stability of the RSPLL with the phase-noise suppression of injection locking. As a result, it achieves an integrated RMS jitter of 92.6 fs and FoM_1/FoM_2 of -253 dB/-266.8 dB, outperforming prior PLL-based ILCMs in both noise and power efficiency. Owing to the stable type-I loop and compact loop-filter design, the proposed architecture maintains fast locking and low power within a small core area. These results demonstrate that the RS-ILPLL offers a compact, low-power, and structurally stable solution among PLL-based ILCMs.

IV. CONCLUSION

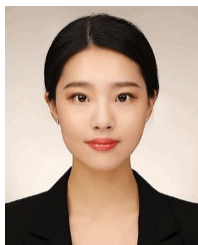
This paper presents a type-I reference-sampling PLL (RSPLL) that, for the first time, incorporates an injection

locking technique for low-jitter clock generation. The proposed RS-ILPLL leverages the wide lock range and inherent stability of the RSPLL while utilizing injection locking to further suppress VCO noise, overcoming the -20 dB/dec suppression slope of the type-I loop. An RSPD-based calibration loop is also introduced to align the injection timing with the PLL path delay. Fabricated in 65-nm CMOS process, the prototype achieves 92.6 fs RMS jitter and locks within 1.3 μ s. The resulting FoM of -253 dB validates the proposed architecture's superior jitter-power efficiency.

REFERENCES

- [1] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.
- [2] B. M. Helal, C.-M. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.
- [3] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.
- [4] C.-F. Liang and K.-J. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2011, pp. 90–92.
- [5] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, "Design and analysis of low-power high-frequency robust sub-harmonic injection-locked clock multipliers," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3160–3174, Dec. 2015.
- [6] Y.-C. Huang and S.-I. Liu, "A 2.4GHz sub-harmonically injection-locked PLL with self-calibrated injection timing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2012, pp. 338–340.
- [7] A. Elkholy, A. Elmallah, M. G. Ahmed, and P. K. Hanumolu, "A 6.75–8.25-GHz -250 -dB FoM rapid ON/OFF fractional- N injection-locked clock multiplier," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1818–1829, Jun. 2018.
- [8] S. Yoo, S. Choi, Y. Lee, T. Seong, Y. Lim, and J. Choi, "A low-jitter and low-reference-spur ring-VCO-based injection-locked clock multiplier using a triple-point background calibrator," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 298–309, Jan. 2021.
- [9] S. Choi, S. Yoo, Y. Lim, and J. Choi, "A PVT-robust and low-jitter ring-VCO-based injection-locked clock multiplier with a continuous frequency-tracking loop using a replica-delay cell and a dual-edge phase detector," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1878–1889, Aug. 2016.
- [10] N. Fujii, S. Morishita, T. Kihara, and T. Yoshimura, "A 2.6 GHz subharmonically injection-locked PLL with low-spur and wide-lock-range injection," in *Proc. 14th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Vancouver, BC, Canada, Jun. 2016, pp. 1–4.
- [11] Z. Zhang, L. Liu, and N. Wu, "A novel 2.4-to-3.6 GHz wideband subharmonically injection-locked PLL with adaptively-aligned injection timing," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Kao Hsiung, Taiwan, Nov. 2014, pp. 369–372.
- [12] M.-S. Choo, H.-G. Ko, S.-Y. Cho, K. Lee, and D.-K. Jeong, "An optimum injection-timing tracking loop for 5-GHz, 1.13-mW/GHz RO-based injection-locked PLL with 152-fs integrated jitter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 12, pp. 1819–1823, Dec. 2018.
- [13] X. Jin, W. Park, D.-S. Kang, Y. Ko, K.-W. Kwon, and J.-H. Chun, "A 4-GHz sub-harmonically injection-locked phase-locked loop with self-calibrated injection timing and pulsewidth," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2724–2733, Oct. 2020.
- [14] A. T. Narayanan, M. Katsuragi, K. Kimura, S. Kondo, K. K. Tokgoz, K. Nakata, W. Deng, K. Okada, and A. Matsuzawa, "A fractional- N sub-sampling PLL using a pipelined phase-interpolator with an FoM of -250 dB," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1630–1640, Jul. 2016.
- [15] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N^2 ," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec. 2009.

- [16] J.-H. Seol, K. Choo, D. Blaauw, D. Sylvester, and T. Jang, "Reference oversampling PLL achieving -256 -dB FoM and -78 -dBc reference spur," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 2993–3007, Oct. 2021.
- [17] Z. Yang, Y. Chen, P.-I. Mak, and R. P. Martins, "A calibration-free, reference-buffer-free, type-I narrow-pulse-sampling PLL with -78.7 -dBc REF spur, -128.1 -dBc/Hz absolute in-band PN and -254 -dB FOM," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 494–497, 2020.
- [18] D.-H. Yoon, D.-K. Jung, K. Seong, J.-S. Han, K.-Y. Chung, J.-E. Kim, T. T. Kim, and K.-H. Baek, "A 3.2-GHz 178-fs_{rms} jitter subsampling PLL/DLL-based injection-locked clock multiplier," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 7, pp. 915–925, Jul. 2022.
- [19] C.-Y. Lin, Y.-T. Hung, and T.-H. Lin, "A 2.4-GHz 500- μ W 370-fs_{rms} integrated jitter sub-sampling sub-harmonically injection-locked PLL in 90-nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 91–94.
- [20] S.-Y. Cho, S. Kim, M.-S. Choo, H.-G. Ko, J. Lee, W. Bae, and D.-K. Jeong, "A 2.5–5.6 GHz subharmonically injection-locked all-digital PLL with dual-edge complementary switched injection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 2691–2702, Sep. 2018.
- [21] D. Liao, Y. Zhang, F. F. Dai, Z. Chen, and Y. Wang, "An mm-wave synthesizer with robust locking reference-sampling PLL and wide-range injection-locked VCO," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 536–546, Mar. 2020.
- [22] T. Xu, S. Zhong, J. Yin, P.-I. Mak, and R. P. Martins, "A 6-to-7.5-GHz 54-fs_{rms} jitter type-II reference-sampling PLL featuring a gain-boosting phase detector for in-band phase-noise reduction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 12, pp. 4774–4786, Dec. 2022.
- [23] J. Sharma and H. Krishnaswamy, "A 2.4-GHz reference-sampling phase-locked loop that simultaneously achieves low-noise and low-spur performance," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1407–1424, May 2019.
- [24] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.
- [25] Keysight. (2013). *E4440A PSA Spectrum Analyzer, 3 Hz to 26.5 GHz*. Datasheet. [Online]. Available: <https://www.keysight.com/us/en/assets/>
- [26] H. Choi and S. Cho, "A 7.5-GHz subharmonic injection-locked clock multiplier featuring a $120\times$ multiplying factor and 92.3-fs RMS jitter including reference spur," *IEEE J. Solid-State Circuits*, vol. 59, no. 12, pp. 3928–3937, Dec. 2024.



JOOHEE LEE (Member, IEEE) received the B.S. degree in electronics engineering from the School of Electronics Engineering, Tech University of Korea (TUKorea), South Korea, in 2020, and the M.S. degree in intelligent semiconductor engineering from Chung-Ang University (CAU), South Korea, in 2025. She is currently with Dongwoon Anatech, Seoul, South Korea. Her research interests include low-noise phase-locked loops (PLLs) and mixed-signal integrated circuit design.



JAE-SOUB HAN (Member, IEEE) received the B.S. and M.S. degrees from the School of Electrical and Electronics Engineering, Chung-Ang University (CAU), Seoul, South Korea, in 2019 and 2021, respectively, where he is currently pursuing the Ph.D. degree in intelligent semiconductor engineering. His research interests include high-speed direct digital frequency synthesizer (DDFS) and low-power phase-locked loop (PLL).



JONGHYUN SEO (Member, IEEE) received the B.S. degree in electrical engineering from Chung-Ang University (CAU), Seoul, South Korea, in 2022, where he is currently pursuing the Ph.D. degree in intelligent semiconductor engineering. His research interest includes frequency synthesizer design.



DONG-HYUN YOON (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical and Electronics Engineering, Chung-Ang University (CAU), Seoul, South Korea, in 2014, 2016, and 2020, respectively. From 2021 to 2023, he was with Nanyang Technological University, Singapore, as a Research Fellow. In 2024, he joined Samsung Electronics, South Korea, as a Staff Engineer. His research interests include high-resolution high-speed digital-to-analog converters (DAC) and direct digital frequency synthesizers (DDS). He is also interested in low-noise phase.



KWANG-HYUN BAEK (Senior Member, IEEE) received the B.S. and M.S. degrees from Korea University, Seoul, South Korea, in 1990 and 1998, respectively, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC), IL, USA, in 2002. From 2000 to 2006, he was a Senior Scientist at the Department of High-Speed Mixed-Signal ICs, Rockwell Scientific Company, formerly Rockwell Science Center (RSC), Thousand Oaks, CA, USA. At RSC, he was involved in the development of high-speed data converters (ADC/DAC) and direct digital frequency synthesizers (DDFS). He was also with Samsung Electronics, from 1990 to 1996. Since 2006, he has been with the School of Electrical and Electronics Engineering, Chung-Ang University (CAU), Seoul, where he is currently a Faculty Member. His research interests include high-performance analog and digital circuits such as high-resolution ADCs, high-speed DACs, hybrid frequency synthesizers (PLLs and DDFSs), high-speed interface circuits (CDRs and SerDes), PMIC, and low-power circuits.

...