

Article

A Calibration-Free Fractional-N PLL with a Time-Averaged Current DAC for High Linearity

Seungjae Kang, Dooweon Kim, Mireu Choi , Jonghyeon Seo and Kwang-Hyun Baek *

Department of Intelligent Semiconductor Engineering, Chung-Ang University, Seoul 06974, Republic of Korea

* Correspondence: kbaek@cau.ac.kr

Abstract

This paper proposes a calibration-free Type-II fractional-N PLL that achieves high linearity by employing a time-averaged current DAC. By adopting a time-averaged current DAC, the proposed architecture inherently enables calibration-free operation and achieves superior linearity, successfully overcoming the fundamental limitations of conventional DTC- and PI-based approaches. The proposed time-averaged current DAC consists of two G_m cells and a variable pulse-width generator. Interpolation is achieved by controlling the injection time of the G_m cells' output currents, effectively performing time-averaging between two current levels. By performing interpolation in the time domain instead of using conventional analog DAC implementations, the proposed approach simplifies the design and achieves improved linearity. The combination of the 3-bit time-averaged current DAC and the quad-phase divider reduces the quantization noise by 24 dB. The proposed PLL is designed in a 65 nm process. Simulation results show that it consumes 3.41 mW of power with a 25 MHz reference frequency and achieves an RMS jitter of 231.8 fs, integrated from 1 kHz to 100 MHz, and a figure-of-merit (FoM_N) of -267.1 dB.

Keywords: phase-locked loop; fractional-N; frequency synthesizer; calibration-free; low phase noise; low power

1. Introduction

Frequency synthesizers are essential components in modern wireless communication systems, requiring both fine frequency resolution and low phase noise. Fractional-N PLLs have been widely adopted due to their ability to achieve fine frequency resolution. However, fractional operation inherently introduces additional noise sources, such as quantization noise and spurious tones, which degrade phase noise performance. In general, reducing jitter requires a wider loop bandwidth to suppress VCO noise, but in fractional-N PLLs, the loop bandwidth is often limited by quantization noise, making it difficult to fully exploit this advantage. To enable a wider loop bandwidth, various techniques have been proposed to suppress quantization noise in fractional-N PLLs. Among them, the use of a digital-to-time converter (DTC) has been widely studied to cancel quantization noise in the time domain [1,2]. Owing to its high resolution, the DTC allows a wider loop bandwidth and enables the use of a high-gain phase detector. However, it typically requires a calibration loop to compensate for PVT variations, and achieving a wide delay range makes the design challenging. Another approach employs a pipelined time-domain phase interpolator (PI) [3]. Although inverter-based PIs can operate without calibration, they suffer from severe linearity degradation due to PVT variations and mismatch, and often require high power consumption. As a calibration-free alternative,



Academic Editor: Fabian Khateb

Received: 19 April 2026

Revised: 22 May 2026

Accepted: 27 May 2026

Published: 1 June 2026

Copyright: © 2026 by the authors.

Licensee MDPI, Basel, Switzerland.

This article is an open access article distributed under the terms and

conditions of the [Creative Commons](https://creativecommons.org/licenses/by/4.0/)[Attribution \(CC BY\)](https://creativecommons.org/licenses/by/4.0/) license.

DAC-based approaches have been proposed, as in [4,5]. Unlike DTC-based architectures, where the fractional control word is converted into an absolute delay and delay-gain error directly produces residual fractional phase error, DAC-based architectures perform relative interpolation between two adjacent phase samples. As DAC-based interpolation relies on the relative current ratio between adjacent phase samples rather than on an absolute delay gain, it relaxes the sensitivity to gain error and eliminates the need for DTC-like gain error calibration. In this work, a time-averaged current DAC is proposed. The proposed DAC consists of two G_m cells and a variable pulse width generator, and performs DAC operation by controlling the injection time of the output currents, effectively achieving time-averaging between two current levels. The proposed time-averaging technique offers two distinct advantages over conventional analog DACs: it significantly reduces hardware complexity by eliminating the need for bulky analog current sources, and it inherently guarantees high linearity by precise time-domain division of a long reference period. This paper is organized as follows. Section 2 describes the overall architecture and operation of the proposed PLL, along with the circuit implementation of each block. Section 3 presents the noise analysis of each block. Simulation results and conclusions are given in Sections 4 and 5, respectively.

2. Proposed Fractional-N PLL Architecture and Design

The overall architecture of the proposed PLL based on the time-averaged current DAC, which achieves fractional-N operation by controlling the pulse width of the output currents, is shown in Figure 1. The output of the LC-VCO is first divided by two to generate quadrature phases I , Q , IB , and QB . The quad-phase divider synchronizes the MMD output with the I , Q , IB , and QB signals to generate signals P_I , P_Q , P_{IB} , P_{QB} , and P_{ID} , spaced by $\frac{1}{2}T_{VCO}$ (0° , 90° , 180° , 270° , and 360°). For phase wrapping operation, the output of a third-order DSM is accumulated by a 5-bit phase accumulator, and the carry output controls the division ratio of the MMD. A multiplexer selects one of two adjacent phases to generate the sampling edges (ϕ_1 , ϕ_2), and the two most significant bits ($S[4:3]$) of the phase accumulator are used as the selection signals.

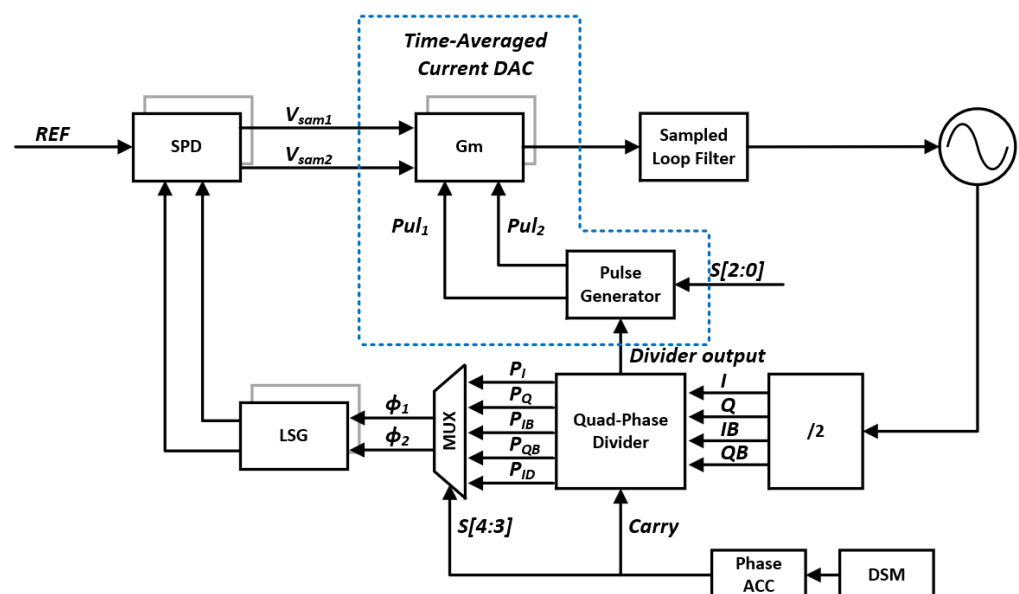


Figure 1. Block diagram of the proposed time-averaged current DAC based fractional-N PLL.

The phase difference between the reference edge and the selected sampling edges (ϕ_1 , ϕ_2) is detected by two identical LSG/SPDs (linear slope generator/sampling PD). Two LSG/SPD circuits generate the sampled voltages V_{sam1} and V_{sam2} , which are propor-

tional to the phase difference. The sampled voltages are then applied to the G_m cells, where they are converted into output currents. When Pul_1 or Pul_2 are high, the current sources in the G_m cells inject currents into the loop filter. Let τ_1 and τ_2 denote the pulse widths of Pul_1 and Pul_2 , respectively. The average current is determined by these pulse widths. Specifically, each G_m cell injects current of $g_{m1}(V_{sam1} - V_{ref})$ and $g_{m2}(V_{sam2} - V_{ref})$ for durations of τ_1 and τ_2 , respectively. As a result, the average output current of the G_m cells is determined by the time-weighted combination of the two currents, effectively achieving interpolation between adjacent phase samples. The pulse widths τ_1 and τ_2 are generated based on the least significant 3 bits ($S[2 : 0]$) of the phase accumulator. This operation realizes fractional phase generation in the charge domain without requiring additional analog interpolation circuitry. By controlling τ_1 and τ_2 , the proposed structure performs time-averaging between two discrete phase points, thereby suppressing quantization noise and improving linearity. Consequently, fine phase resolution is achieved while maintaining a simple and calibration-free implementation. Finally, a sampled loop filter is used, as in [6], to minimize spurs caused by current pulses injected into the loop filter by the G_m cells.

2.1. LSG and SPD Circuit

The LSG and SPD circuits adopt the structure in [3]. Their schematic and operating waveforms are shown in Figure 2a,b, respectively. When REF is low and ϕ is high, both C_{sam} and C_{dum} are discharged to ground through M_1 . At the rising edge of REF , M_1 turns off and the current source I_1 starts charging C_{sam} and C_{dum} . Because a constant current I_1 charges a capacitance $C_{sam} + C_{dum}$, the node voltages increase linearly with a slope of $\frac{I_1}{C_{sam} + C_{dum}}$. When ϕ falls, the switch (SW) opens. At this moment, V_{sam} is sampled, while V_{dum} continues to increase. At the falling edge of REF , M_1 turns on again and discharges V_{dum} to ground. Finally, when ϕ rises, SW turns on and resets V_{sam} to ground, preparing the circuit for the next cycle. In the proposed PLL, two identical LSG/SPDs detect the phase differences between the reference edge and the sampling edges (ϕ_1 and ϕ_2). The resulting voltages are denoted as V_{sam1} and V_{sam2} . V_{sam1} and V_{sam2} are then applied to the G_m cells, as shown in Figure 1. The G_m cells inject current only after V_{sam} has settled, so no additional hold operation is required in the SPD.

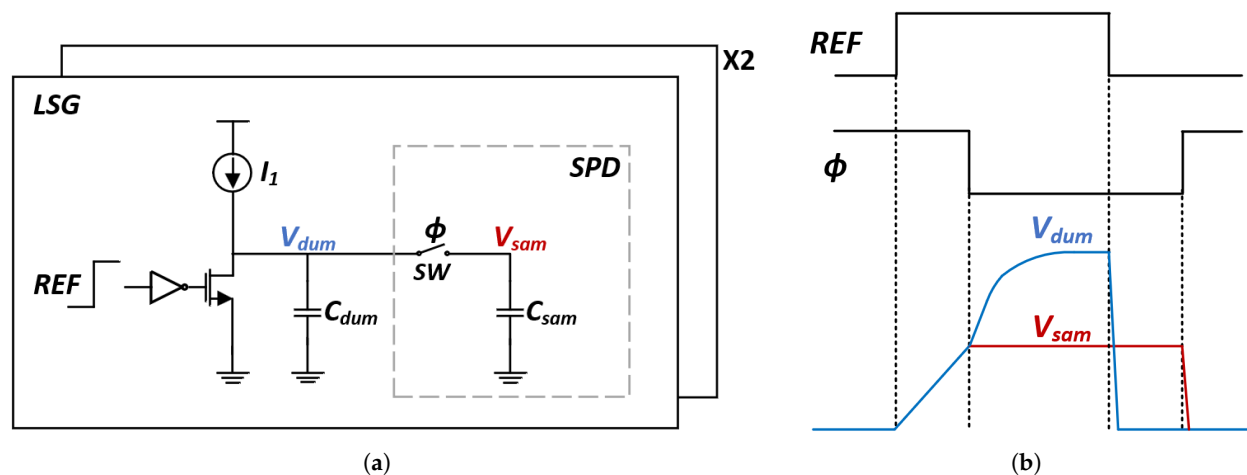


Figure 2. (a) Schematic of LSG/SPD. (b) Sampling operation waveform.

2.2. G_m Cells and Time-Averaged Current DAC

The schematics of the two G_m cells are shown in Figure 3. Two identical G_m cells convert the sampled voltages V_{sam1} and V_{sam2} into output currents proportional to their differences from V_{ref} . The reference voltage V_{ref} is set to $\frac{V_{DD}}{3}$ so that the LSG operates within its linear region when the PLL is locked, and G_{m1} and G_{m2} are designed to be

equal. When Pul is high and $\overline{Pul}$ is low, the UP and DN current sources of the G_m cells are connected to the loop filter and inject current into the loop filter. Pul_1 and Pul_2 are designed as non-overlapping pulses.

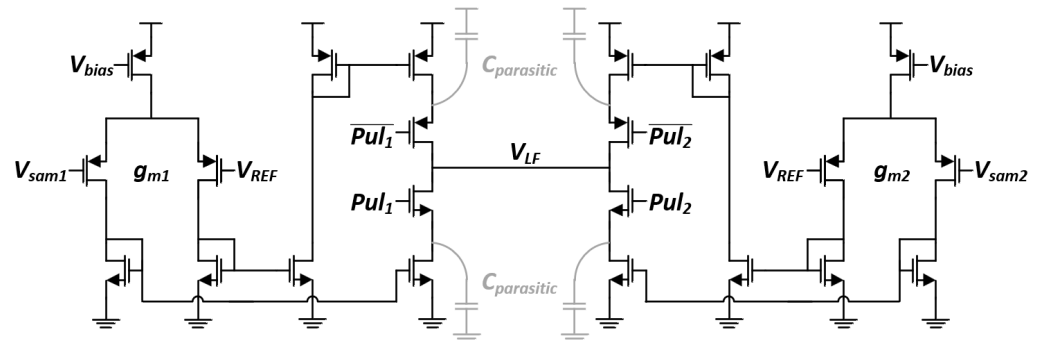


Figure 3. Schematic of G_m cells.

The proposed time-averaged current DAC is realized by the combination of the two G_m cells and the pulse signals Pul_1 and Pul_2 . The pulse signals are generated by a pulse generator using the divided VCO frequency. Let τ_s denote the pulse width step. Then, τ_1 and τ_2 can be expressed as

$$\tau_1 = (8 - \alpha)\tau_s \quad (1)$$

$$\tau_2 = \alpha\tau_s \quad (2)$$

where α ranges from 0 to 7 and is controlled by the least significant 3 bits, $S[2:0]$, of the phase accumulator. Let I_1 and I_2 denote the currents injected into the loop filter by the two G_m cells. As $g_{m1} = g_{m2} = g_m$, the currents are given by

$$I_1 = (V_{sam1} - V_{ref})g_m \quad (3)$$

$$I_2 = (V_{sam2} - V_{ref})g_m \quad (4)$$

The average output current over the current injection interval $\tau_1 + \tau_2$ is then given by

$$I_{avg, \tau_1 + \tau_2} = \frac{I_1\tau_1 + I_2\tau_2}{\tau_1 + \tau_2} = \frac{I_1(8 - \alpha)\tau_s + I_2\alpha\tau_s}{8\tau_s} = \frac{8 - \alpha}{8}I_1 + \frac{\alpha}{8}I_2 \quad (5)$$

Therefore, by adjusting the value of α , the proposed time-averaged current DAC can generate an average current between I_1 and I_2 . This operation yields an average current equivalent to the weighted summation of current sources in a current DAC [4], under the same total current injection time. It should be noted that $I_{avg, \tau_1 + \tau_2}$ in (5) is defined as the average current over the current injection interval $\tau_1 + \tau_2$. The effective average current delivered to the loop filter over one reference period includes the duty factor $(\tau_1 + \tau_2)/T_{ref}$ and is given by

$$I_{avg, ref} = I_{avg, \tau_1 + \tau_2} \frac{\tau_1 + \tau_2}{T_{ref}} = \frac{I_1\tau_1 + I_2\tau_2}{T_{ref}}. \quad (6)$$

Figure 4 further illustrates the operation of the proposed time-averaged current DAC. For example, when $\alpha = 0$, the average current over $\tau_1 + \tau_2$ is equal to I_1 . When $\alpha = 1$, I_1 is injected into the loop filter for $7\tau_s$, while I_2 is injected for τ_s . The resulting average current over $\tau_1 + \tau_2$ is $\frac{7}{8}I_1 + \frac{1}{8}I_2$. This behavior can be generalized for all values of α , where the output current is interpolated between I_1 and I_2 with a resolution of $\frac{1}{8}$. Consequently, the proposed structure effectively realizes a 3-bit current DAC in the time domain, achieving current interpolation without requiring additional analog current sources. The 3-bit resolution was selected for fair comparison with the DAC-based architectures in [4].

The maximum INL target was set below 0.1 LSB for improved linearity over [4]. As the interpolation is performed in the time domain using digital pulse control over a reference period, the proposed approach achieves improved linearity.

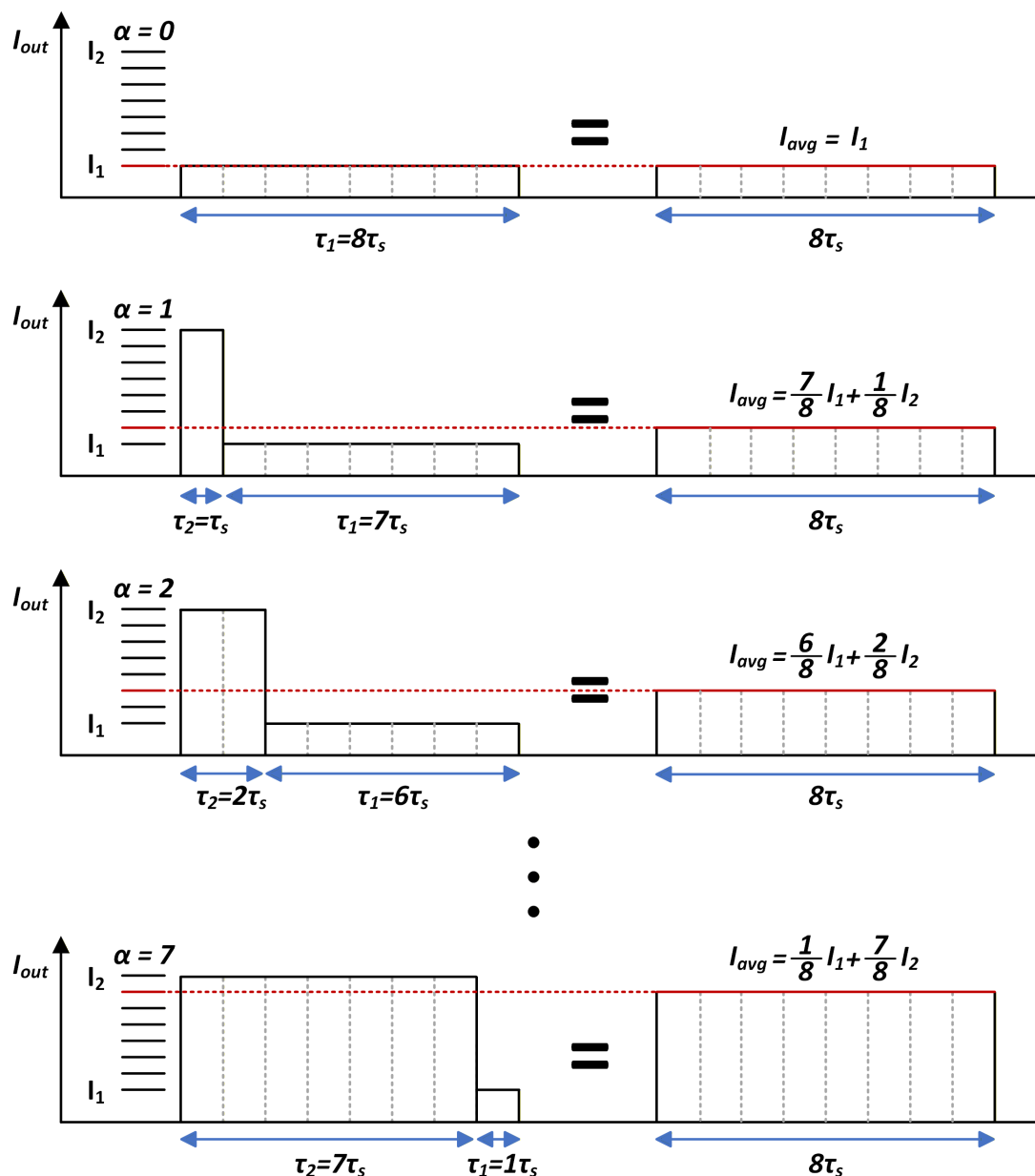


Figure 4. Proposed time-averaged current DAC operation waveform. The red dashed line represents the average current level.

However, in the proposed structure, when Pul is low and the switch is open, the drain nodes of the current sources are charged to V_{DD} for the PMOS and to ground for the NMOS. When the switch turns on, charge sharing occurs between these nodes and the loop filter capacitor, leading to current distortion. This results in degraded linearity of the proposed current DAC. While a unity-gain amplifier could suppress this effect [7], it incurs a severe power penalty. To address this trade-off, we employ an energy-efficient current dumping technique inspired by [8]. This approach pre-charges the drain node, effectively resolving the charge sharing issue without the need for power-hungry active amplifiers. However, when the $\overline{Pul}$ signal is used to inject current into the dumping node as in [8], V_{LF} and V_{dump} are not equal. This is because the average current injected into C_{dump} differs from that

injected into the loop filter. Therefore, a modified current injection scheme is required for the dumping node in the proposed structure. The final G_m cells structure with improved charge sharing is shown in Figure 5. In each G_m cell, an additional current path to C_{dump} is introduced, and the current is steered to C_{dump} when the Pul_D signal is high. The operation of the proposed structure is illustrated in Figure 6a.

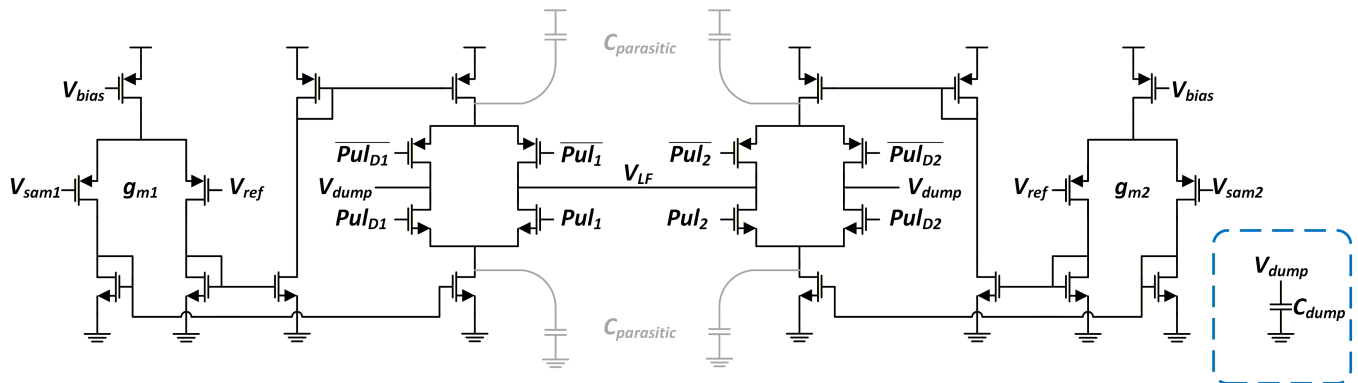


Figure 5. Schematic of the G_m cells with improved charge sharing. The blue dashed frame indicates the current dumping path connected to V_{dump} .

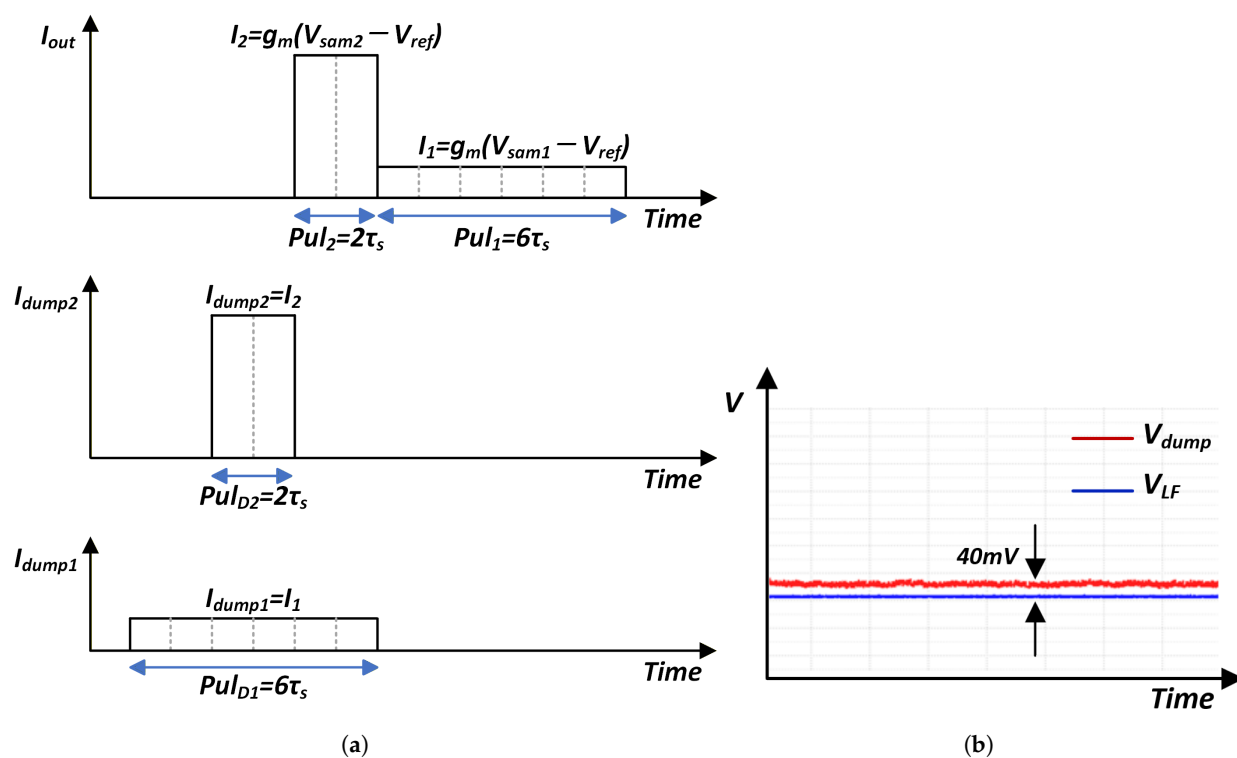


Figure 6. (a) G_m cells operation waveform with the proposed charge sharing reduction structure. (b) Simulated voltage of V_{LF} and V_{dump} .

Before the main current is injected into the loop filter, auxiliary pulses Pul_D with the same pulse widths as Pul are used to inject the same amount of current into C_{dump} . In this way, the voltage at C_{dump} follows the loop filter voltage (V_{LF}) and pre-charges the drain node of the current source to the same level. For example, when $\alpha = 2$, Pul_1 and Pul_2 operate in the same manner as in Figure 4, injecting an average current of $\frac{6}{8}I_1 + \frac{2}{8}I_2$ into the loop filter. The auxiliary pulses Pul_{D2} and Pul_{D1} have the same pulse widths as Pul_2 and Pul_1 , respectively. Pul_{D1} injects I_1 into C_{dump} for a duration of $\tau_1 = 6\tau_s$, while Pul_{D2} injects I_2 into C_{dump} for $\tau_2 = 2\tau_s$. Therefore, the total injected current into C_{dump} is identical to that

injected into the loop filter over the same period. In steady state, the net charge delivered to the loop filter and C_{dump} is zero, and the voltage at C_{dump} (V_{dump}) closely follows the loop filter voltage (V_{LF}) due to channel length modulation. Moreover, Pul_D remains high until the Pul signal is applied, keeping the drain node of the current source at V_{dump} prior to the main current injection. As a result, the drain node is pre-charged to the loop filter voltage, thereby significantly reducing charge sharing and improving linearity.

The simulated voltages at the V_{dump} and V_{LF} nodes are shown in Figure 6b. The steady-state offset between V_{dump} and V_{LF} is mainly caused by parasitic capacitance mismatch at the PMOS and NMOS current source drain nodes. Before the auxiliary dumping pulse Pul_D turns on, the PMOS drain node is charged to V_{DD} , whereas the NMOS drain node is discharged to ground. Thus, when Pul_D turns on, the capacitance mismatch between the two drain nodes introduces an additional charge error into V_{dump} , resulting in the steady-state offset between V_{dump} and V_{LF} . The impact of this offset on the DAC linearity is further analyzed in Section 2.2.2.

Another design consideration is the selection of the pulse width step τ_s . If the pulse width of Pul is too short, the drain node of the current source does not have sufficient time to settle to V_{dump} , which still causes distortion in the output current. Therefore, in this work, the pulse width step τ_s is set to $4T_{VCO}$ to ensure sufficient settling time. The reference frequency is also set to 25 MHz to provide sufficient current injection time within each reference period.

2.2.1. Analytical Linearity Modeling of the Time-Averaged Current DAC

To analytically explain the linearity behavior of the proposed time-averaged current DAC, the average current is modeled by considering charge sharing induced current error, G_m mismatch, and timing related non-idealities. For the 3-bit interpolation, the pulse widths τ_1 and τ_2 are determined by the interpolation code α as

$$\tau_1 = (8 - \alpha)\tau_s \quad (7)$$

$$\tau_2 = \alpha\tau_s \quad (8)$$

where τ_s is the pulse width step. Therefore, the total current injection time is kept constant as

$$\tau_{tot} = \tau_1 + \tau_2 = 8\tau_s \quad (9)$$

The ideal average current delivered to the loop filter over one reference period can be expressed as

$$I_{avg,ideal}(\alpha) = \frac{I_1\tau_1 + I_2\tau_2}{T_{ref}} = \frac{\tau_s}{T_{ref}}[(8 - \alpha)I_1 + \alpha I_2] \quad (10)$$

where I_1 and I_2 are the output currents of the two G_m cells. As $\tau_{tot} = 8\tau_s$ is constant, the ideal average current changes linearly with the interpolation code. In practical implementation, the residual average-current error can be decomposed into several error components as

$$\Delta I_{res}(\alpha) = \Delta I_{CS}(\alpha) + \Delta I_{G_m}(\alpha) + \Delta I_{\tau}(\alpha) \quad (11)$$

where ΔI_{CS} , ΔI_{G_m} , and ΔI_{τ} represent the residual errors due to charge sharing, G_m mismatch, and timing related non-idealities, respectively.

The current domain errors caused by charge sharing and G_m mismatch can be modeled as current errors during the two pulse intervals. In addition, timing related non-idealities, such as pulse edge jitter and duty cycle distortion, can be modeled as effective pulse width

errors. When both current domain errors and time domain errors are included, the actual average current over one reference period can be written as

$$I_{avg,real}(\alpha) = \frac{(I_1 + \Delta I_1)(\tau_1 + \Delta \tau_1) + (I_2 + \Delta I_2)(\tau_2 + \Delta \tau_2)}{T_{ref}} \quad (12)$$

where ΔI_1 and ΔI_2 represent the current errors during τ_1 and τ_2 , respectively, and $\Delta \tau_1$ and $\Delta \tau_2$ represents the effective pulse width errors.

The residual average current error is then given by

$$\Delta I_{res}(\alpha) = I_{avg,real}(\alpha) - I_{avg,ideal}(\alpha) \quad (13)$$

$$\Delta I_{res}(\alpha) = \frac{\Delta I_1 \tau_1 + \Delta I_2 \tau_2 + I_1 \Delta \tau_1 + I_2 \Delta \tau_2 + \Delta I_1 \Delta \tau_1 + \Delta I_2 \Delta \tau_2}{T_{ref}} \quad (14)$$

As ΔI_1 and ΔI_2 are small current perturbations and $\Delta \tau_1$ and $\Delta \tau_2$ are small timing perturbations, the product terms $\Delta I_1 \Delta \tau_1$ and $\Delta I_2 \Delta \tau_2$ are much smaller than the first-order error terms. Therefore, these terms can be neglected, and the residual average current error can be approximated as

$$\Delta I_{res}(\alpha) \simeq \frac{\Delta I_1 \tau_1 + \Delta I_2 \tau_2}{T_{ref}} + \frac{I_1 \Delta \tau_1 + I_2 \Delta \tau_2}{T_{ref}} \quad (15)$$

The first term represents the current domain residual error caused by charge sharing and G_m mismatch, while the second term represents the time domain residual error caused by pulse width errors. These pulse width errors mainly originate from the VCO timing variation used in the pulse generator. Even under free-running VCO conditions, the resulting timing error is expected to be only on the order of a few *ps*, which is much smaller than the minimum pulse width τ_s of approximately 1.67 ns. As ΔI is a few μA , the time domain error term $I \Delta \tau / T_{ref}$ is approximately two orders of magnitude smaller than the current-domain error term $\Delta I \tau / T_{ref}$ under this design condition. Therefore, the time domain residual error is negligible compared with the current domain residual error. Consequently, the residual average current error is dominated by the current domain term and can be simplified as

$$\Delta I_{res}(\alpha) \simeq \frac{\Delta I_1 \tau_1 + \Delta I_2 \tau_2}{T_{ref}} \quad (16)$$

The INL is then obtained by normalizing this residual error to the ideal LSB current:

$$INL(\alpha) = \frac{\Delta I_{res}(\alpha)}{I_{LSB}} \quad (17)$$

where the ideal LSB current over one reference period is defined as

$$I_{LSB} = \frac{\tau_s}{T_{ref}} (I_2 - I_1) \quad (18)$$

Based on this residual error model, the proposed time-averaged current DAC is designed to keep the maximum INL below 0.1 LSB. The charge sharing induced current error is identified as the dominant residual error, which is further verified through the V_{dump} offset sweep and Monte Carlo simulations. The corresponding simulation results are discussed in detail in the following paragraphs.

2.2.2. Linearity Verification of the Proposed Time-Averaged Current DAC

Figure 7a shows the linearity of the time-averaged current DAC with and without the charge sharing reduction structure for a typical simulation run. The structure with the

current dumping node shows much better linearity than the one without it, confirming that the proposed charge sharing reduction structure effectively suppresses the current domain residual error. The INL degradation is mainly observed at DAC codes 001 and 111, where one of the pulse widths becomes the minimum value of τ_s . It is meaningful to analyze the change in DAC linearity according to the offset between V_{dump} and V_{LF} . Figure 7b shows the simulated INL for different offsets between V_{dump} and V_{LF} . When the offset is large, the charge sharing reduction structure cannot effectively suppress the charge sharing effect. As a result, the INL increases over the entire DAC code range. When the offset decreases, the overall charge sharing induced error is reduced, and the residual INL degradation is mainly observed at DAC codes 001 and 111. This indicates that, after the offset between V_{dump} and V_{LF} is sufficiently reduced, the DAC linearity is primarily limited by the insufficient pre-charging time of the current source drain node. In this work, the offset is designed to remain below 50 mV, which is sufficient to meet the target INL requirement. To reduce the offset, the PMOS current source is sized to match the NMOS parasitic capacitance, at the cost of voltage headroom. The lengths of the current source are selected by considering the area-matching trade-off and the required output resistance, which leads to an increase in the drain node parasitic capacitance.

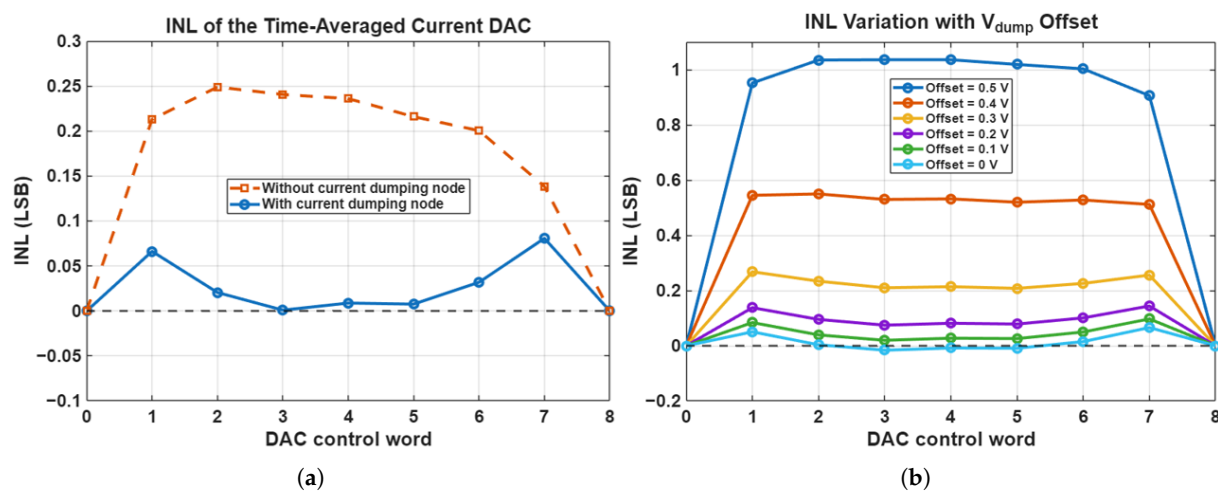


Figure 7. (a) INL of proposed time-averaged current DAC for a typical simulation run. (b) INL variation with V_{dump} offset.

In this work, the two G_m cells are implemented with a carefully symmetric layout to minimize mismatch. Nevertheless, mismatch between the two G_m cells produces unequal transconductance values. In the proposed time-averaged current DAC, the interpolated average current is determined by the weighted combination of the two G_m outputs. Therefore, the G_m mismatch appears as a code-dependent current error and can degrade the linearity, resulting in INL degradation and potentially increasing fractional spurs. To verify the robustness of the DAC-based interpolation against device mismatch, Monte Carlo simulations were performed with mismatch variations applied to the two G_m cells.

As shown in Figure 8, the simulated maximum INL remains within 0.0923 LSB within the 3σ range over 200 Monte Carlo runs, demonstrating that the DAC-based interpolation maintains sufficient linearity under G_m cell mismatch. In each Monte Carlo run, the maximum INL occurs at codes 001 and 111, indicating that the maximum INL is mainly dominated by charge sharing induced current distortion rather than by G_m cell mismatch.

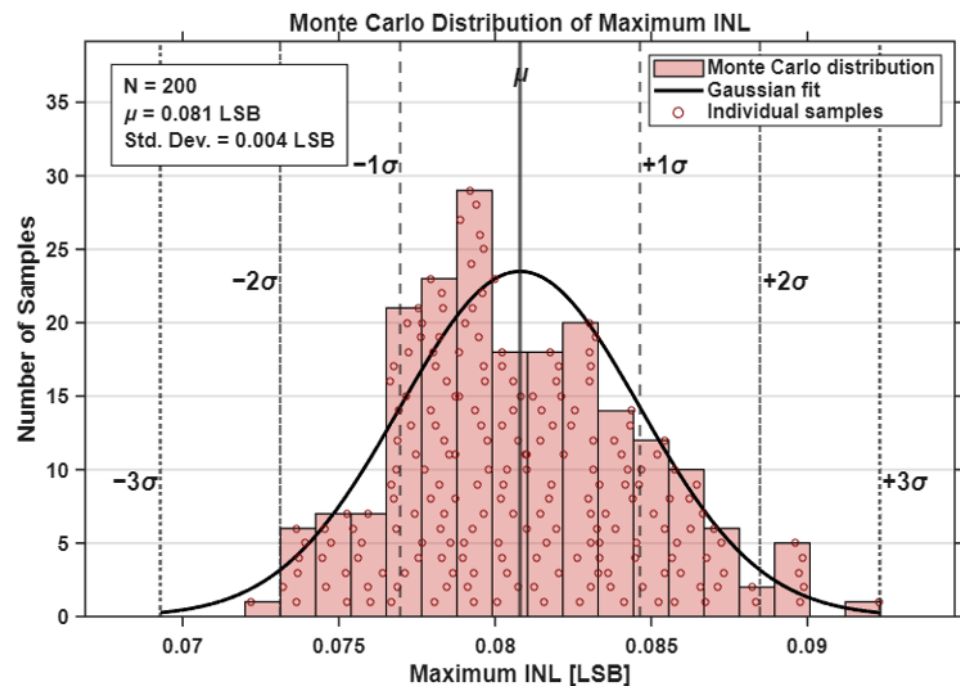


Figure 8. Monte Carlo simulation results for the maximum INL in the time-averaged current DAC.

2.3. Quad-Phase Divider and Pulse Generator

The MMD circuit is shown in Figure 9. The MMD is implemented by cascading 2/3 divider cells, as in [9]. When an input signal with a frequency of $\frac{F_{VCO}}{2}$ (denoted as F_0) is applied, F_0 is divided according to the division ratio selected by MC. The resulting output frequency is denoted as F_5 and is used in the quad-phase divider. In addition, the MMD generates another output, Mod_0 , with the same division ratio and a pulse width of $2T_{VCO}$, which is used in the pulse generator.

The quad-phase divider is shown in Figure 10. The operation of the quad-phase divider is as follows. A frequency divide-by-2 receives the VCO output and generates quadrature phases I , Q , IB , and QB with a spacing of $\frac{1}{2}T_{VCO}$. These signals are then used to synchronize the MMD output F_5 , generating phase signals P_I , P_Q , P_{IB} , P_{QB} , and P_{ID} (corresponding to 0° , 90° , 180° , 270° , and 360°). A multiplexer uses the two most significant bits ($S[4:3]$) of the phase accumulator to select two adjacent phases from P_I to P_{ID} and uses them as the sampling edges (ϕ_1 , ϕ_2) for the LSG/SPD. To generate the pulse signals required for the time-averaged current DAC, a pulse generator is employed, as shown in Figure 11. The pulse generator consists of two main blocks: a shift register that generates multiple delayed pulse edges and a pulse selection block that selects the rising and falling edges of the output pulses. The shift register is clocked by QB and generates a pulse sequence with a constant edge spacing of $2T_{VCO}$.

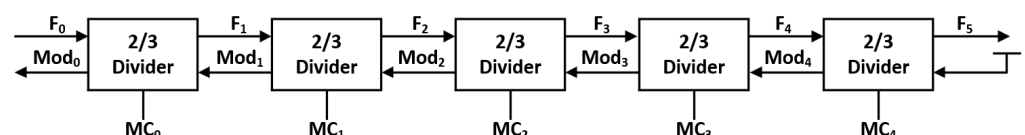


Figure 9. Schematic of multi modulus divider.

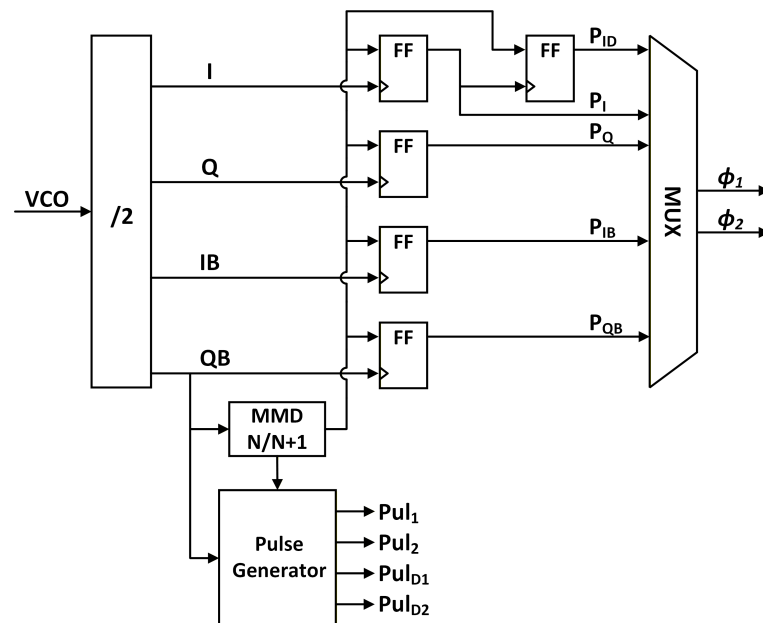


Figure 10. Schematic of quad-phase divider.

The operation of the shift register is as follows. The Mod_0 signal is first aligned with the rising edge of QB in the MMD. It is then sampled at the falling edge of QB by the first flip-flop of the shift register to generate $P[0]$. The shift register then shifts $P[0]$ through each stage with a delay of $2T_{VCO}$ per flip-flop, driven by the falling edge of QB . This process generates the pulse sequence $P[0]$ to $P[30]$. The corresponding waveform of this operation is shown in Figure 11. The signals $P[0]$ to $P[30]$ are used in the pulse selection block to control the pulse widths of Pul_1 , Pul_2 , Pul_{D1} , and Pul_{D2} .

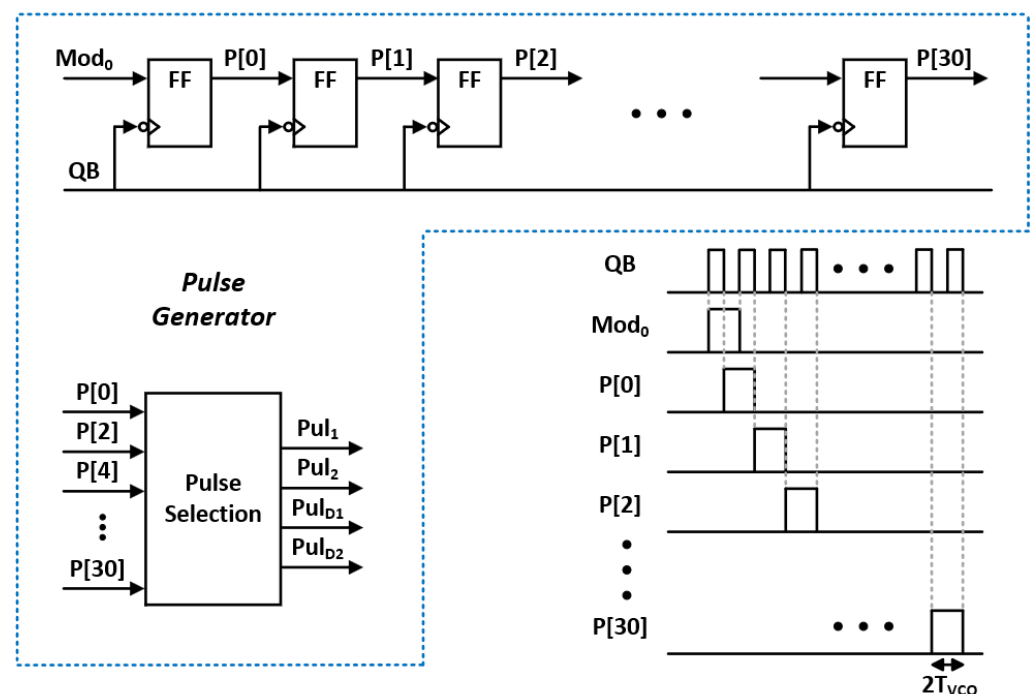


Figure 11. Schematic of pulse generator.

As shown in Figure 12a, the pulse selection block consists of multiplexers and SR latches, and its operating waveform is illustrated in Figure 12b. The multiplexers select two pulses from the delayed pulse sequence $P[n]$ and apply them to the S and R inputs of the

SR latch. As the pulse step is set to $4T_{VCO}$, only even-indexed pulses among $P[n]$ are used as inputs to the multiplexer. The rising edge of the S-input pulse determines the rising edge of the latch output, while the rising edge of the R-input pulse determines the falling edge. The selection signals of the multiplexer are determined by the least significant 3 bits ($S[2:0]$) of the phase accumulator to generate the desired pulse width. For example, when $S[2:0] = 010$, the rising edge of Pul_1 is aligned with the rising edge of $P[16]$. The falling edge is aligned with $P[20]$, resulting in a pulse width of $2\tau_s = 8T_{VCO}$. The remaining signals, Pul_2 , Pul_{D1} , and Pul_{D2} , are generated in the same manner, as illustrated in Figure 6a.

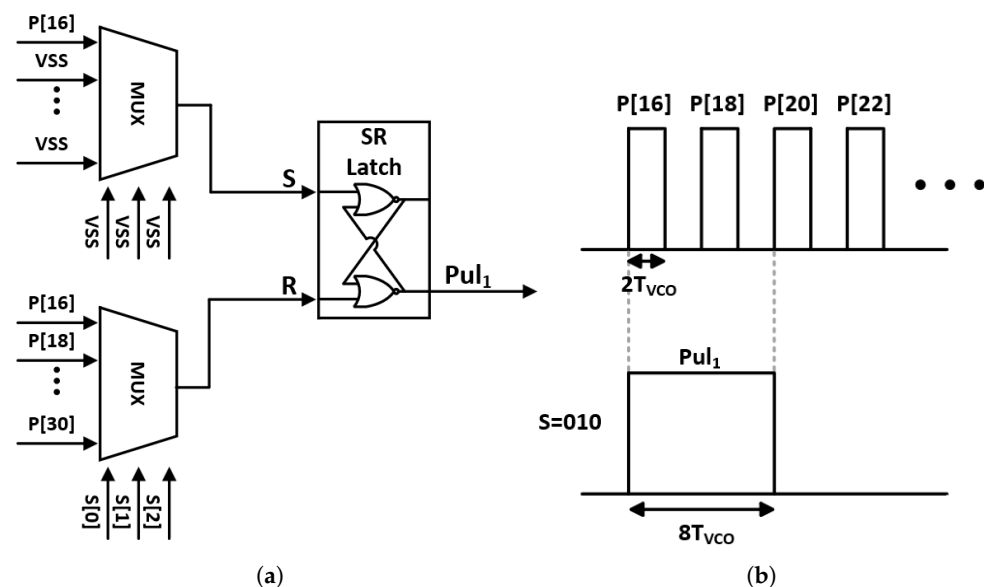


Figure 12. (a) Schematic of pulse selection block. (b) Waveform of pulse selection block.

2.4. Sampled Loop Filter

When the proposed time-averaged current DAC operates, different currents from the two G_m cells are injected into the loop filter, which causes voltage variation at V_{LF} and increases spurious tones. To minimize these spurs, a sampled loop filter structure, as in [6], is used, and its schematic is shown in Figure 13. The capacitor C_s is divided into two equal capacitors with a switch between them. When the EN signal is high, C_1 is connected to the rest of the loop filter. The switch is implemented using a transmission gate with a dummy switch to reduce charge injection. When current is injected from the G_m cells, the switch is open, and C_1 integrates the current. After the current injection ends, the voltage on C_1 settles. Then, the switch is closed to allow charge sharing between C_1 and the rest of the loop filter. As a result, voltage variation is prevented from directly propagating to the loop filter, which suppresses spur components.

To quantify the contribution of the sampled loop filter, the fractional spur was compared with and without the sampled loop filter. When the sampled loop filter is enabled, the fractional spur is further reduced by approximately 1 dB. Compared to [10], which employs a wide loop bandwidth, the sampled loop filter has a smaller impact in this work, as the narrow loop bandwidth already sufficiently attenuates the fractional spur.

Even under this condition, the sampled loop filter further suppresses the residual fractional spur that remains after the loop-dynamics attenuation. Thus, it serves as an auxiliary spur suppression mechanism that offers additional design margin and robustness.

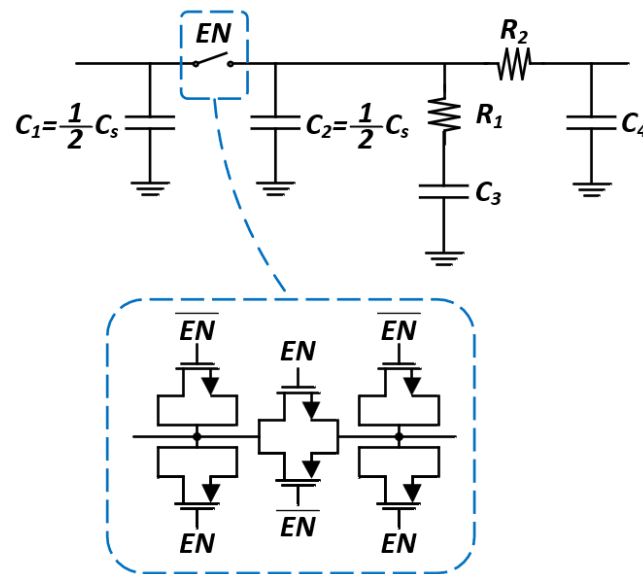


Figure 13. Schematic of sampled loop filter.

2.5. LC-VCO

The schematic of the LC-VCO is shown in Figure 14. An NMOS and PMOS cross-coupled pair structure is used in the LC-VCO due to its power efficiency. The VCO covers a frequency range of 2.3–2.5 GHz, and K_{VCO} is designed to be approximately 50 MHz/V. A 5-bit capacitor bank provides discrete coarse frequency tuning to cover the desired frequency range under PVT variations. The proposed PLL targets 2.4 GHz ISM-band wireless applications, such as Bluetooth-like low-power wireless transceivers.

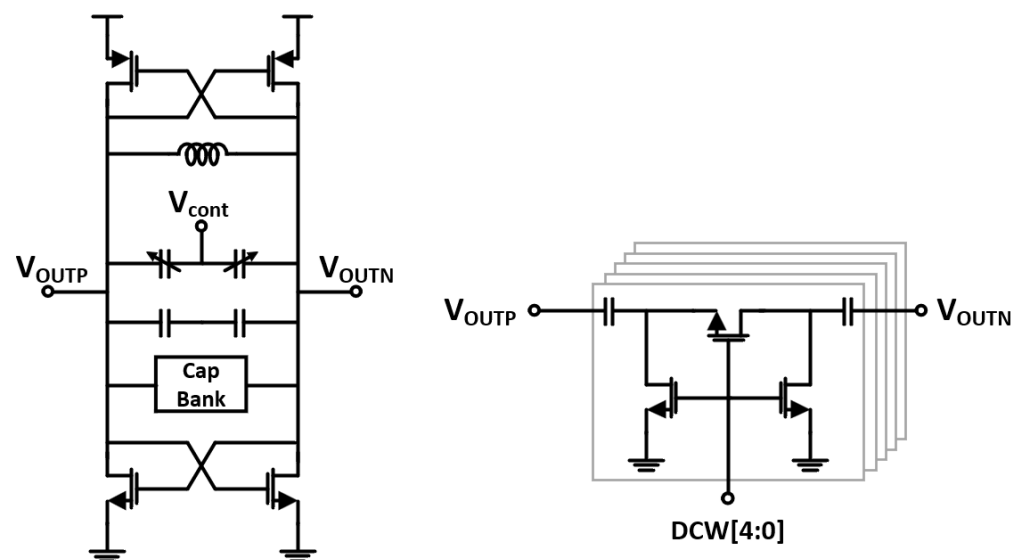


Figure 14. Schematic of the LC-VCO.

3. Noise Analysis of the Proposed Architecture

In this section, the noise contributions of each block are analyzed. The linearized phase-domain model of the proposed PLL is shown in Figure 15.

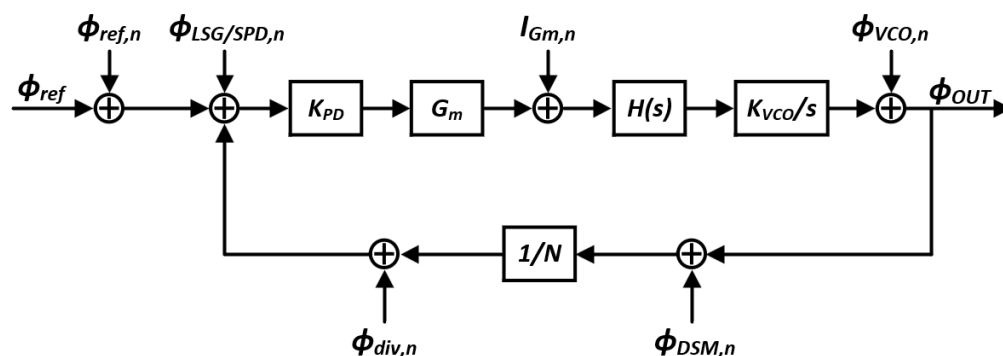


Figure 15. Linearized phase-domain model of proposed PLL.

3.1. G_m Cells Noise

The noise and feedback gain of the proposed G_m cells are the same as those of a single G_m cell with a pulser in [3]. Unlike [4], the currents of G_{m1} and G_{m2} do not change with the DAC code. As each G_m cell injects current only during its pulse width within one reference period, the effective noise contribution includes the corresponding duty factor. Only the injection time changes with the DAC code. The thermal noise spectral density of each G_m cells is given as follows.

$$S_{i,Gm1} = 8kT\gamma g_{m1} \frac{\tau_1}{T_{ref}} \quad (19)$$

$$S_{i,Gm2} = 8kT\gamma g_{m2} \frac{\tau_2}{T_{ref}} \quad (20)$$

k is Boltzmann's constant and T is the absolute temperature. $S_{i,Gm1}$ and $S_{i,Gm2}$ represent the thermal noise spectral densities of G_{m1} and G_{m2} , respectively. As $g_{m1} = g_{m2} = g_m$ and the total injection time τ_{tot} is given by $\tau_1 + \tau_2$, the overall noise spectral density of the G_m cells can be expressed as follows.

$$S_{i,Gm} = 8kT\gamma g_m \frac{\tau_{tot}}{T_{ref}} \quad (21)$$

This corresponds to the noise of a single G_m cell with a current injection time of τ_{tot} . Similarly, the feedback gain of the G_m cells can be written as follows.

$$\beta_{Gm} = \frac{\Delta i_{Gm}}{\Delta \phi_{VCO}} = \frac{\frac{\Delta \phi_{DIV}}{2\pi} T_{ref} S_l g_m}{\Delta \phi_{VCO}} \frac{\tau_{tot}}{T_{ref}} = \frac{S_l g_m \tau_{tot}}{2\pi N} \quad (22)$$

The factor τ_{tot}/T_{ref} accounts for the duty factor of the pulsed G_m cell operation, so the effective G_m cell gain seen by the loop filter is scaled by this duty factor. The in-band noise contribution of the G_m cells can be calculated as follows using (21) and (22).

$$\mathcal{L}_{in-band,Gm} = \frac{1}{2} S_{i,Gm} \left| \frac{1}{\beta_{Gm}} \right|^2 = \frac{16kT\gamma\pi^2 N^2}{T_{ref} S_l^2 g_m \tau_{tot}} \quad (23)$$

G_m cell-induced noise can be reduced by increasing G_m through higher current consumption. In this work, $\tau_{tot} = 13.2$ ns, $S_l = 300$ MV/s, $N = 96$, and $g_m = 0.33$ mS, and the in-band noise due to the G_m cells is -108 dBc/Hz, making it the dominant noise source in the in-band region.

3.2. LSG/SPD Noise

The noise contribution of the LSG/SPD is evaluated by converting the voltage noise on C_{sam} into the corresponding phase error at the divider output in steady state.

$$\overline{v_{SPD,n}^2} = \frac{kT}{C_{sam}} = \left(S_l \frac{\Delta\phi_{DIV,SPD}}{2\pi} T_{ref} \right)^2 \quad (24)$$

As $\Delta\phi_{VCO} = N\Delta\phi_{DIV}$, this can be written in terms of the VCO phase error as follows.

$$\overline{v_{SPD,n}^2} = \frac{kT}{C_{sam}} = \left(S_l \frac{\Delta\phi_{VCO,SPD}}{2\pi N} T_{ref} \right)^2 \quad (25)$$

$$\Delta\phi_{VCO,SPD}^2 = \frac{kT}{C_{sam}} \left(\frac{2\pi N}{S_l T_{ref}} \right)^2 \quad (26)$$

As the LSG/SPD samples at f_{ref} , the in-band phase noise is limited to $\frac{f_{ref}}{2}$. The in-band phase noise due to the LSG/SPD can be calculated as follows.

$$2\mathcal{L}_{in-band,SPD} \frac{f_{ref}}{2} = \Delta\phi_{VCO,SPD}^2 \quad (27)$$

By substituting (26) for $\Delta\phi_{VCO}$, the expression can be written as follows.

$$\mathcal{L}_{in-band,SPD} = \left(\frac{2\pi N}{S_l} \right)^2 \frac{kT}{C_{sam}} \frac{1}{T_{ref}} = \left(\frac{2\pi}{S_l} \right)^2 \frac{kT}{C_{sam}} T_{ref} f_{VCO}^2 \quad (28)$$

In the LSG/SPD design, increasing S_l reduces the LSG/SPD-induced noise. However, S_l is limited by the requirement to ensure the linearity of the G_m cell at the selected sampling edge. Although increasing the capacitance can also reduce the LSG/SPD-induced noise, a larger current is required to maintain the same S_l . In this circuit, $T_{ref} = 40$ ns, $C_{sam} = C_{hold} = 150$ fF, and $f_{VCO} = 2.4$ GHz. The in-band phase noise of the LSG/SPD is -116 dBc/Hz and can be considered negligible.

3.3. DSM and Divider Noise

Quantization noise power can be expressed as

$$\sigma_q^2 = \frac{\Delta^2}{12} \quad (29)$$

where Δ is the quantization step size. When the step size is reduced by a factor of M , the resulting quantization noise power becomes

$$\sigma_{q,1/M}^2 = \frac{(\Delta/M)^2}{12} = \frac{\Delta^2}{12M^2} = \frac{\sigma_q^2}{M^2} \quad (30)$$

Therefore, reducing the quantization step size by a factor of M suppresses the quantization-noise power by $20\log_{10}(M)$ dB. In the proposed architecture, the quad-phase divider generates phase edges from 0° to 360° with a spacing of $T_{VCO}/2$. The two adjacent edges are then selected and further interpolated by the time-averaged current DAC with 3-bit resolution. Therefore, the proposed architecture is equivalent to dividing one T_{VCO} period into 16 phase steps, as in [3]. Therefore, quantization noise is reduced by $20\log_{10}(16) \approx 24$ dB compared to a conventional fractional-N PLL. In addition, the phase noise of the divider is negligible because the divider output is retimed by a D flip-flop.

4. Simulation Results

The proposed fractional-N PLL is designed in a 65 nm CMOS process with a 1 V supply, and the layout of the chip is shown in Figure 16a. The total power consumption is 3.41 mW, and the power consumption of each block is summarized in Table 1. Figure 16b shows the simulated output spectrum in fractional-N mode. The simulated in-band phase noise is -108 dBc/Hz, and the reference spur is -89.6 dBc, while the fractional spur is

−65.1 dBc with the sampled loop filter. The loop bandwidth is approximately 200 kHz, and the RMS jitter, integrated from 1 kHz to 100 MHz, is 231 fs. Table 2 compares the proposed PLL with other calibration-free fractional-N PLLs. In conventional fractional-N PLLs, a lower reference frequency generally acts as a performance penalty. However, in the proposed architecture, the 25 MHz reference frequency also offers a design benefit. It provides a larger timing margin for the pulse-width operation of the time-averaged current DAC, thereby improving DAC linearity. Nevertheless, for a given output frequency, the lower reference frequency increases the division ratio and can degrade the phase noise performance. As the jitter-power FoM does not include the effect of the division ratio, FoM_N is also reported in this work. The works in [4,5] employ 3-bit DAC-based interpolation and achieve high linearity. Compared with the DAC-based approaches in [4,5] this work shows a lower jitter-power FoM due to the use of a low reference frequency. However, when evaluated using FoM_N , the proposed PLL is comparable to those designs. Moreover, the proposed time-averaged current DAC reduces hardware complexity compared with the DAC-based approaches in [4,5] and is less sensitive to device mismatch and PVT variations.

Table 1. Power breakdown.

Block	Power Consumption (mW)
VCO	1.62
LSG/SPD	0.23
G_m cells	0.47
DSM	0.18
Pulse generator/Divider	0.91

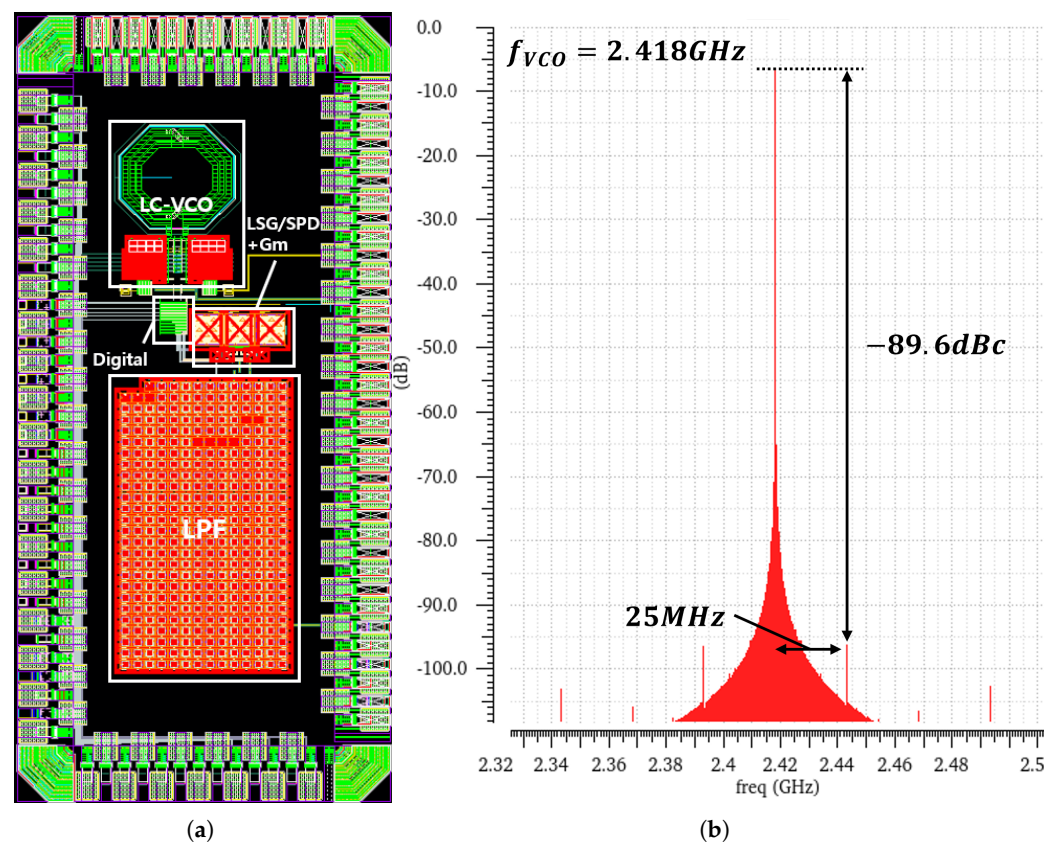


Figure 16. (a) Layout of proposed PLL. (b) Output spectrum of the proposed PLL.

Table 2. Comparison with calibration-free Fractional-N PLLs.

Ref.	[3] TCAS-1'2019	[4] JSSC'2021	[5] TCAS-2'2025	[10] TCAS-1'2025	This Work *
Process (nm)	130	130	65	40	65
Architecture	Inverter-based PI	DAC-based PICP	Embedded phase interpolation PD	Dual loop phase clamping	Time-averaged current DAC
Out. Freq (GHz)	1.9–2.3	1.8–2.3	5.7–5.9	3	2.3–2.5
Ref. Freq (MHz)	50	50	100	31.25	25
In-band PN (dBc/Hz)	−110 @200 kHz	−106 @200 kHz	−110.4 @150 kHz	N/A	−108.2 @100 kHz
RMS jitter σ_{jitter} (fs) (Integ. range)	291.3 (10 kHz–10 MHz)	414 (N/A)	202 (N/A)	197.8 (N/A)	231.8 § (1 kHz–100 MHz)
Ref. Spur (dBc)	−83	−83	−74.3	−123.6	−89.6
Frac. Spur (dBc)	−48.5	−57	−49.6	−96.6	−65.1
Power (mW)	3.2	2.8	4.8	13.2	3.41
FoM †	−246	−243	−247.1	−242.8	−247.3
FoM_N ‡	−262.4	−259.4	−264.7	−262.6	−267.1

* Simulated, † $FoM = 10\log_{10}(\sigma_{jitter}^2 \times Power/1mW)$, ‡ $FoM_N = FoM + 10\log_{10}\left(\frac{F_{ref}}{F_{VCO}}\right)$, § Estimated from model-ing and circuit-level simulations., N/A: not available from the referenced paper.

5. Conclusions

This paper presents a calibration-free fractional-N PLL using a time-averaged current DAC. The proposed DAC achieves fractional operation by controlling the injection time of the G_m output currents, enabling fine phase control in the time domain without requiring additional analog circuits. Consequently, the proposed time-averaged current DAC architecture provides a highly linear, hardware-efficient, and fully calibration-free solution for high-resolution fractional-N frequency synthesis. By combining the time-averaged current DAC with a quad-phase divider, the effective current resolution is enhanced, leading to a reduction in quantization noise. In addition, a current dumping technique is employed to suppress charge sharing, further improving linearity. The simulation results show that the proposed PLL achieves low fractional spur of −65.1 dBc. The LSG/SPD noise contribution is designed to be negligible, and the overall performance is mainly limited by the G_m cells' noise. Compared with previously reported calibration-free fractional-N PLLs, the proposed design achieves comparable performance while offering improved linearity and reduced quantization noise with a simple and calibration-free architecture.

Author Contributions: Conceptualization, methodology, validation, writing—original draft, S.K.; writing—review and editing, D.K.; investigation, M.C.; software, J.S.; supervision, K.-H.B. All authors have read and agreed to the published version of the manuscript.

Funding: This paper was supported by Korea Planning & Evaluation Institute of Industrial Technology (KEIT) (2410000542, RS-2024-00403483) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea), and National R & D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (RS-2021-NR057239), and the Chung-Ang University Graduate Research Scholarship in 2024.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available upon request from the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Wu, W.; Yao, C.; Guo, C.; Chiang, P.; Chen, L.; Lau, P.; Bai, Z.; Son, S.W.; Cho, T.B. A 14-nm Ultra-Low Jitter Fractional-N PLL Using a DTC Range Reduction Technique and a Reconfigurable Dual-Core VCO. *IEEE J. Solid-State Circuits* **2021**, *56*, 3756–3767. [[CrossRef](#)]
2. Narayanan, A.T.; Katsuragi, M.; Kimura, K.; Kondo, S.; Tokgoz, K.K.; Nakata, K.; Deng, W.; Okada, K.; Matsuzawa, A. A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator with an FoM of -250 dB. *IEEE J. Solid-State Circuits* **2016**, *51*, 1630–1640. [[CrossRef](#)]
3. Tao, J.; Heng, C.-H. A 2.2-GHz 3.2-mW DTC-Free Sampling $\Delta\Sigma$ Fractional-N PLL with -110 -dBc/Hz In-Band Phase Noise and -246 -dB FoM and -83 -dBc Reference Spur. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 3317–3329. [[CrossRef](#)]
4. Su, H.; Tao, J.; Balon, S.D.; Heng, C.-H. A 2.3 GHz 2.8 mW Sampling $\Delta\Sigma$ PLL Achieving -110 dBc/Hz In-Band Phase Noise and 500 MHz FMCW Chirp. *IEEE J. Solid-State Circuits* **2021**, *56*, 3458–3469. [[CrossRef](#)]
5. Wang, Y.; Tao, J.; Heng, C.-H. A 5.8-GHz 4.8-mW -247.1 -dB-FoM DTC-Free Sampling $\Delta\Sigma$ Fractional-N PLL with Embedded Phase Interpolation. *IEEE Trans. Circuits Syst. II Express Briefs* **2025**, *72*, 1832–1836.
6. Wang, K.J.; Swaminathan, A.; Galton, I. Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz Fractional-N PLL. *IEEE J. Solid-State Circuits* **2008**, *43*, 2787–2797. [[CrossRef](#)]
7. Johnson, M.G.; Hudson, E.L. A variable delay line PLL for CPU-coprocessor synchronization. *IEEE J. Solid-State Circuits* **1988**, *23*, 1218–1223. [[CrossRef](#)]
8. Gao, X.; Klumperink, E.A.M.; Socci, G.; Bohsali, M.; Nauta, B. Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector. *IEEE J. Solid-State Circuits* **2010**, *45*, 1809–1821. [[CrossRef](#)]
9. Ren, H.; Huang, Y.; Yang, Z.; Chen, T.; Meng, X.; Yan, W.; Zhang, W.; Li, Z.; Iizuka, T.; Mak, P.; et al. A Type-II Reference-Sampling PLL with Non-Uniform Octuple-Sampling Phase Detector Achieving 55-fs JitterRMS, -91.9 -dBc Reference Spur and -259 -dB Jitter-Power FOM. In *Proceedings of the 2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*; IEEE: New York, NY, USA, 2024; pp. 113–116.
10. Yan, T.; Jiang, J.; Silva-Martinez, J. A Fractional Spur Cancellation Technique for Fractional-N Frequency Synthesizers Enabled by Dual Loop Phase Clamping. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2025**, *72*, 3791–3801. [[CrossRef](#)]

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.