

Article

A Comparator-Less Buck Converter with Fast Transient Response Using a Reactive Ramp Generator

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Abstract: This paper introduces a voltage-mode DC-DC buck converter designed to address the challenges of high-frequency operation. The proposed comparator-less Reactive Ramp Generator (RRG) topology mitigates the issues associated with comparator delays, achieving a fast load transient response. By eliminating all comparators from the buck converter's control circuit, we prevent potential delay-induced malfunctions, thereby enhancing overall operational reliability. The rapid response of the RRG, enabled by a short feedback loop, allows for swift output voltage regulation during load transients. Replacing comparators in the PWM controller with inverters effectively removes delay issues without adding complexity. Since the proposed design retains the conventional voltage-mode transfer function, standard type-3 compensation is readily applicable. Operating with a 3.3 V input, the buck converter provides an output range from 0.65 V to 3.0 V, achieving a settling time of 0.802 μ s for load changes from 200 mA to 1 A, and 1.27 μ s for load changes from 1 A to 200 mA. The proposed architecture achieves a peak efficiency of 92.78% at 2.4 V and 600 mA.

Keywords: buck converter; comparator delay; dc-dc converter; high frequency; inverter; pulse-width modulation (PWM); ramp generator; transient response; voltage-mode control



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1. Introduction

The rising demand for high-speed processors has driven an increase in system power consumption, creating a need for efficient power management solutions. As shown in Figure 1, many processors now employ Dynamic Voltage and Frequency Scaling (DVFS), an effective approach to reducing power consumption by adjusting supply voltage or switching frequency based on application demands [1–4]. A DC-DC converter with a wide output range and fast regulation is essential for supporting DVFS [5–8]. To enable rapid response to varying load currents, a high-frequency buck converter is often preferred [9–18]. High switching frequencies extend bandwidth (typically set at 10–20% of the switching frequency), leading to a faster transient response. Additionally, high-frequency converters allow for the use of smaller inductors and capacitors, reducing system size.

However, high-frequency operation introduces challenges, such as increased switching losses, which scale with frequency and can reduce overall efficiency. Thus, a 30 MHz switching frequency is selected to balance efficiency with fast transient response [9,17,18]. Furthermore, comparator delays within the control loop become a concern at higher frequencies, as even nanosecond-scale delays can result in operational errors, potentially degrading performance.

Various approaches have been developed to address comparator delays in high-frequency converters. For instance, Lin Cheng's method introduces V'_H and V'_L in a feedback loop, reducing the number of passive components to minimize area [9]. Nevertheless, when operating at

30 MHz, duty range limitations and comparator delays remain concerns. Cheng Huang proposed a comparator-less controller based on an error amplifier and delay-line for voltage-to-duty-cycle conversion [10], yet this approach, focused on a single control block, requires further stability verification for the full control loop. Qiwei Huang utilized two voltage-controlled delay lines for PWM signal generation via phase difference analysis, driving a charge pump [11]. However, this approach is sensitive to PVT variations, which impact delay accuracy. Liyan Yi introduced a comparator-free ramp generator using a flipped voltage follower buffer [12], but incorporating a buffer to set the minimum ramp value adds complexity, and bandwidth limitations of the feedback amplifier could hinder performance.

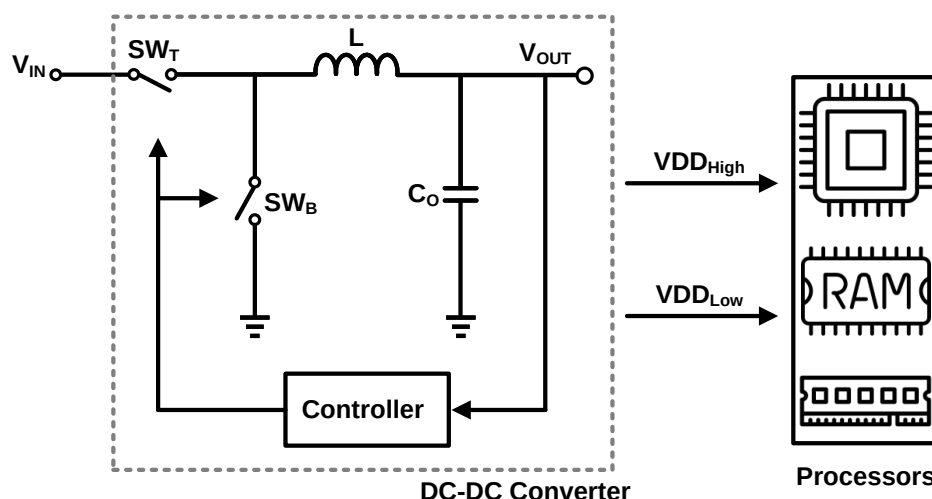


Figure 1. Application of high-frequency buck converter.

Despite these advancements, existing solutions face challenges such as limited duty range, sensitivity to process variations, and stability issues in the full control loop. In this work, we propose a comparator-less Reactive Ramp Generator (RRG) that addresses these problems by offering improved transient response and reduced sensitivity to PVT variations through a novel circuit architecture. By eliminating the comparator and utilizing a Reactive Ramp Generator, the circuit achieves faster transient response while reducing power consumption and complexity. Furthermore, the simplicity of the proposed architecture facilitates integration in compact systems, making it ideal for modern power electronics where space and performance are critical factors. The RRG dynamically adjusts the peak of the ramp signal according to the error amplifier output, reflecting changes in output voltage. This peak-adjusted ramp is inverted to generate the PWM signal, facilitating the desired regulated output. The short feedback loop and quick response of the ramp signal to output voltage changes ensure a fast load transient response.

The remainder of this paper is structured as follows: Section 2 discusses the issues that arise when using conventional buck converter architectures at high frequencies. Section 3 details the proposed high-frequency RRG-based inverter topology. Section 4 presents the experimental results, and Section 5 provides the conclusion.

2. Comparator Delay Issues in Conventional Buck Converters

In a conventional buck converter, shown in Figure 2, comparators play a crucial role in two primary sections: the ramp generator and the PWM controller. As discussed in previous sections, high-frequency operation can cause circuit malfunctions due to comparator delays. This section examines how comparator delays specifically impact the ramp generator and the PWM controller.

In a typical ramp generator, two comparators and an SR latch are employed [19]. This configuration generates a fixed switching frequency f_{sw} and a fixed ramp amplitude V_M , controlled by reference voltages V_H and V_L . Figure 3 illustrates the schematic of a conventional ramp generator and the waveform of V_{RAMP} when comparator delays are present. Here, current I_1 is determined by reference voltage V_{REF} and resistor R_T . As I_1 charges the capacitor C_T , V_{RAMP} increases until it exceeds V_H , at which point C_T is discharged via a switch. Conversely, when V_{RAMP} falls below V_L , the switch is turned off, allowing C_T to recharge. The relationship governing this behavior is defined by

$$f_{sw} = \frac{I_1}{C_T \times V_M} = \frac{V_{REF}}{R_T \times C_T \times (V_H - V_L)} \quad (1)$$

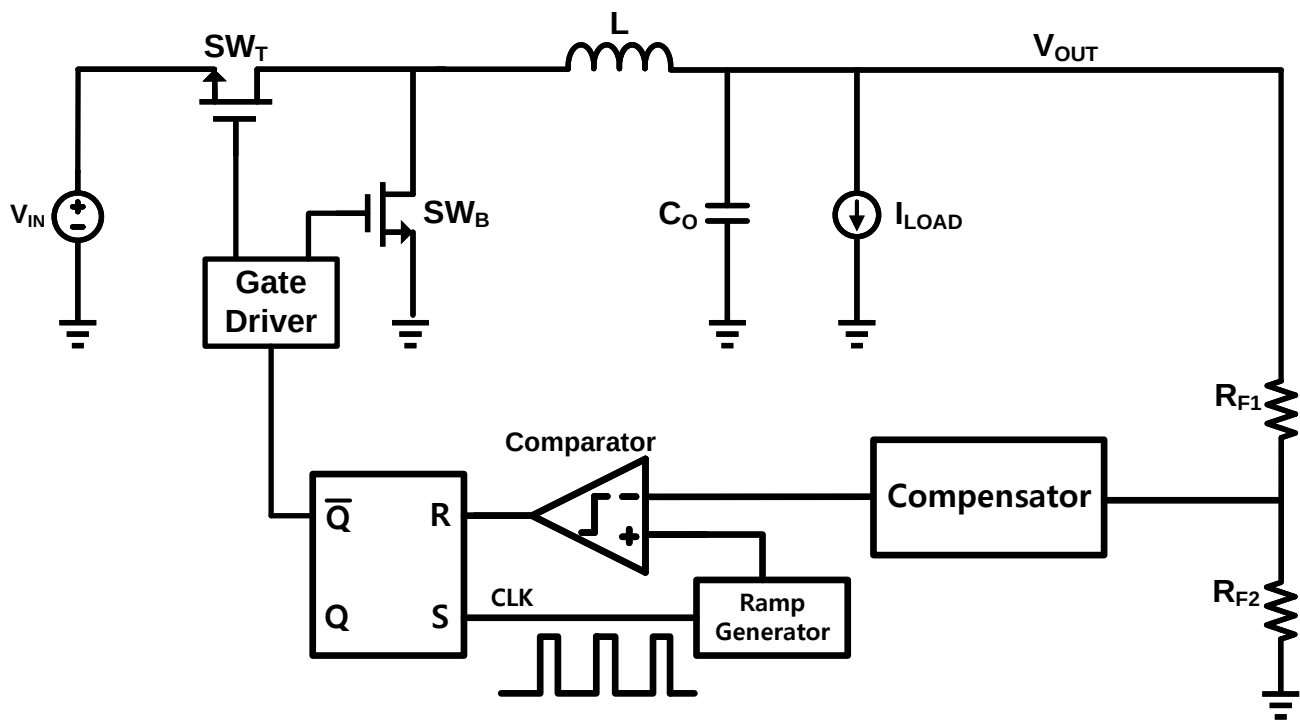


Figure 2. Conventional buck converter.

Comparator delays affect ramp amplitude V_M and switching frequency f_{sw} across a wide range of operating conditions. For instance, at lower frequencies, such as 1 MHz, delays are often negligible because the charging and discharging cycles dominate. However, at higher frequencies (e.g., >10 MHz), even 1 ns delays accumulate, resulting in significant deviations in V_M and reductions in f_{sw} . This issue arises from the fundamental timing mismatch inherent to comparator-based designs. To mitigate these deviations, clamping V_H and V_L to fixed levels may stabilize amplitude V_M to some extent. However, this approach does not address the underlying delay in the comparators, which still results in timing mismatches that distort the switching frequency, particularly at higher frequencies. Figure 4 shows the V_{RAMP} waveform under comparator delays of 0 ns, 1 ns, and 2 ns. In the absence of delay, the ramp oscillates accurately between 0.2 V and 1.25 V, resulting in a ramp amplitude of 1.05 V and a switching frequency of 30.2 MHz. Conversely, delays of 1 ns and 2 ns cause the ramp to deviate from the desired range between V_H and V_L , leading to switching frequencies of 25.6 MHz and 21.8 MHz—decreases of 15% and 28%, respectively.

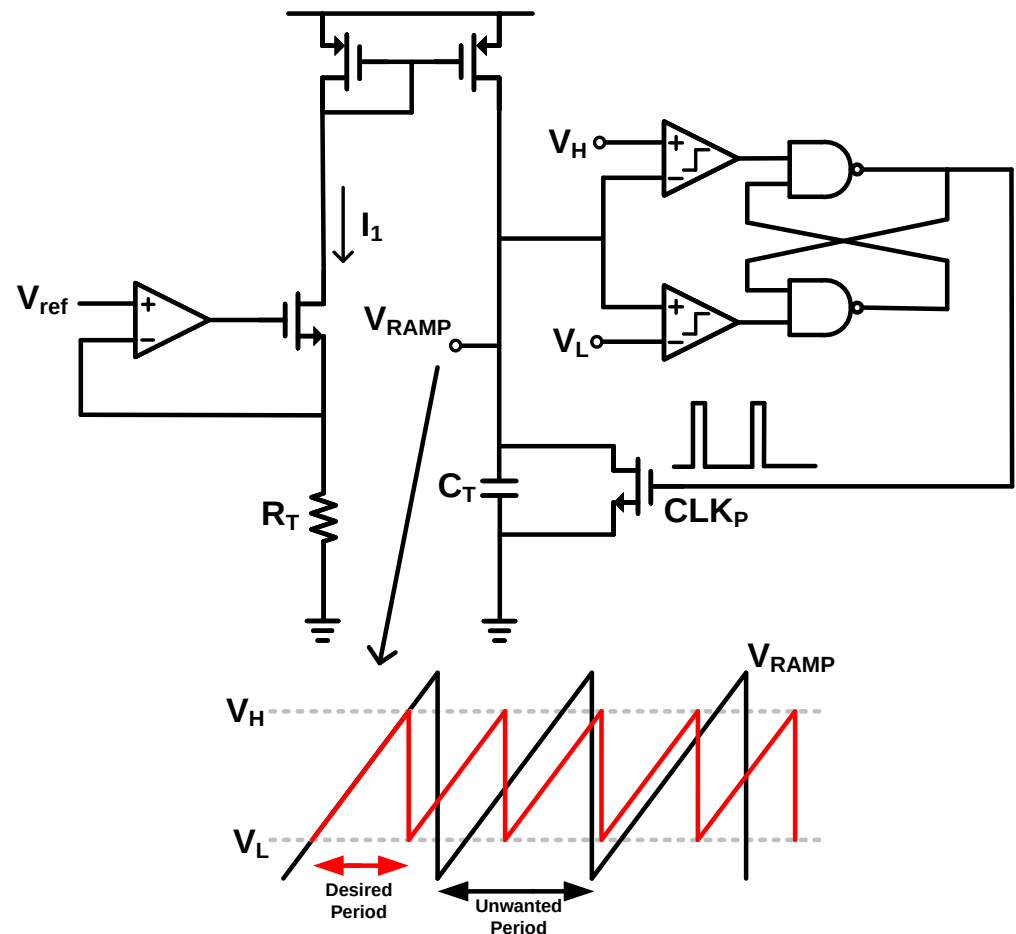


Figure 3. Conventional ramp generator and V_{RAMP} .

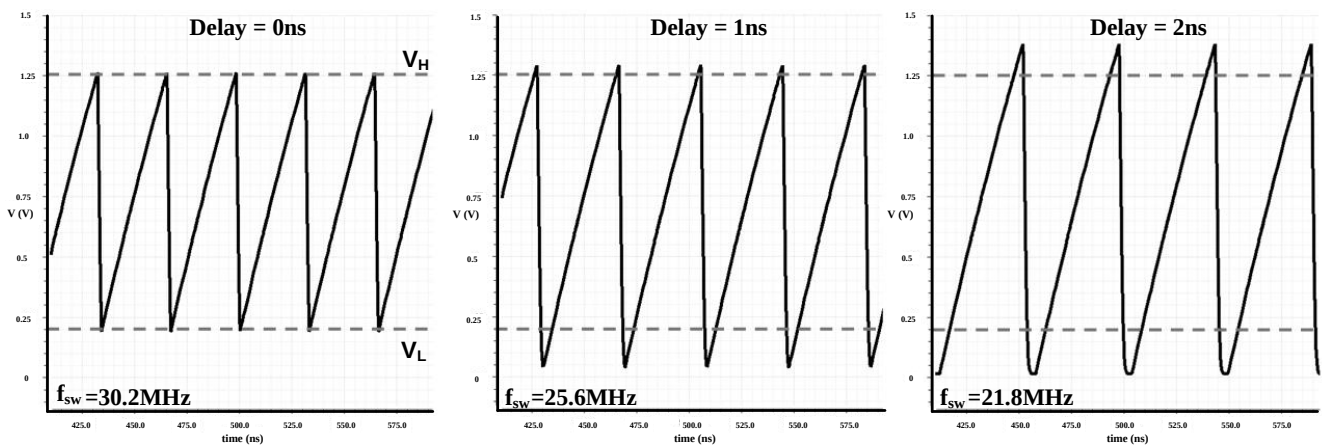


Figure 4. Simulation results of the ramp generator with variable delay on comparators.

The PWM signal generation controller also relies on a comparator. As shown in Figure 5a, an error amplifier processes a scaled-down version of the output voltage, V_{OUT} , represented as bV_{OUT} , and the reference voltage V_{REF} . The error amplifier generates an output voltage, V_{EA} , to balance these inputs. This V_{EA} is then compared with a ramp signal of fixed amplitude V_M through a comparator. The comparator's output serves as the reset input, while the clock pulse from the ramp generator serves as the set input for an SR latch, generating the PWM signal that regulates the output voltage.

However, as illustrated in Figure 5b, comparator delays introduce critical issues. When V_{CMP} , the comparator's output, overlaps with the clock pulse CLK_P , both the set (S) and

reset (R) inputs of the SR latch simultaneously receive a high signal ($S = 1$ and $R = 1$), resulting in a latch violation. This violation disrupts the SR latch's operation, preventing proper PWM signal generation and failing to maintain the desired output voltage.

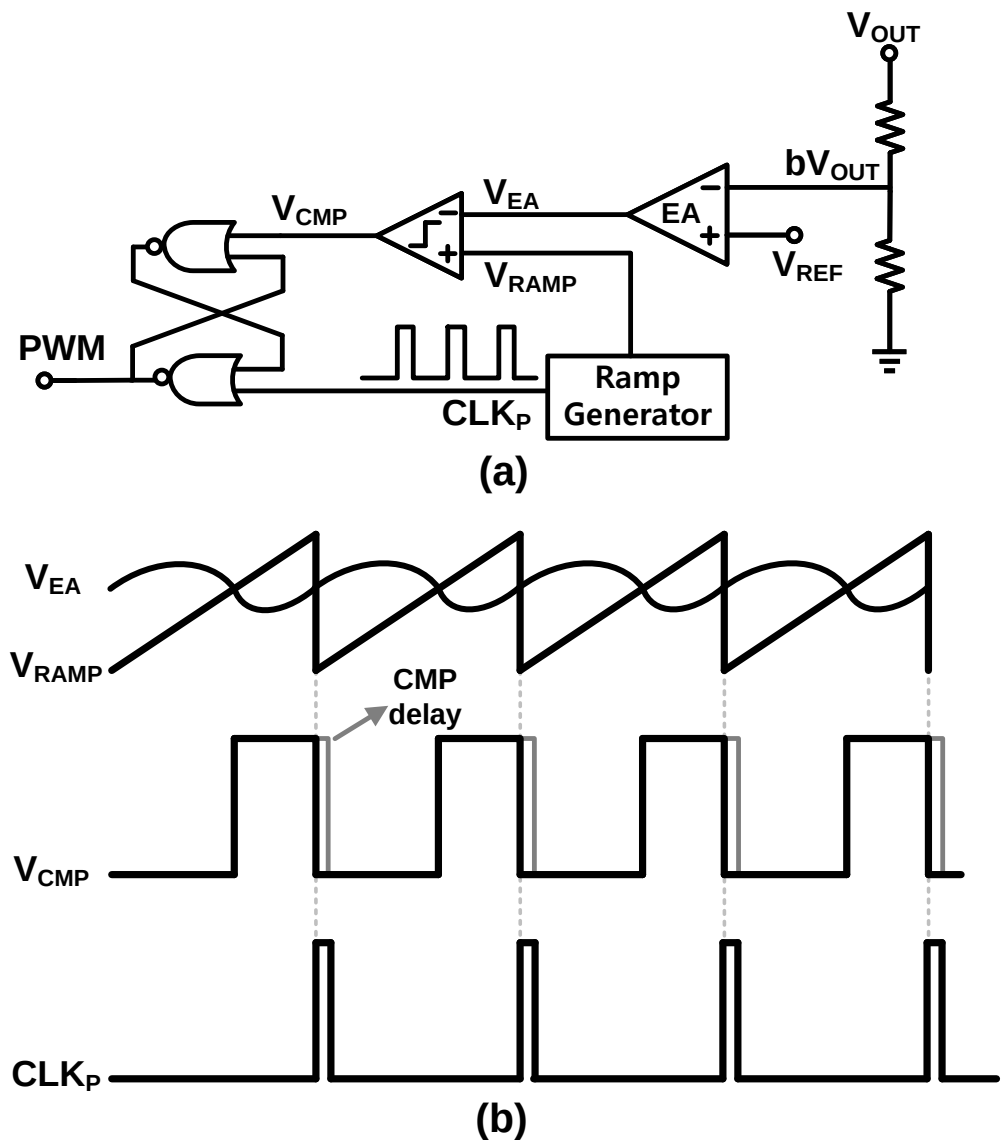


Figure 5. (a) Conventional ramp generator, (b) SR latch violation due to comparator delay.

3. Proposed Reactive Ramp Generator-Based Buck Converter

In this work, we propose a Reactive Ramp Generator (RRG) to address the issues observed in high-frequency buck converters discussed in Section II, while also achieving a fast load transient response. The block diagram of the RRG-based PWM buck converter is shown in Figure 6. In this configuration, the PMOS and NMOS transistors in the power stage switch on and off according to the PWM signal provided by the controller, generating the desired output voltage, V_{OUT} . The output voltage, V_{OUT} , is scaled down by resistors R_{F1} and R_{F2} to produce a signal, bV_{OUT} , which is then processed by the error amplifier to create V_{EA} , ensuring that bV_{OUT} equals V_{REF} . The magnitude of V_{EA} determines the current generated by the RRG, which subsequently affects the peak value of V_{RAMP} . When the V_{RAMP} signal passes through an inverter, a PWM signal is generated to control the output voltage.

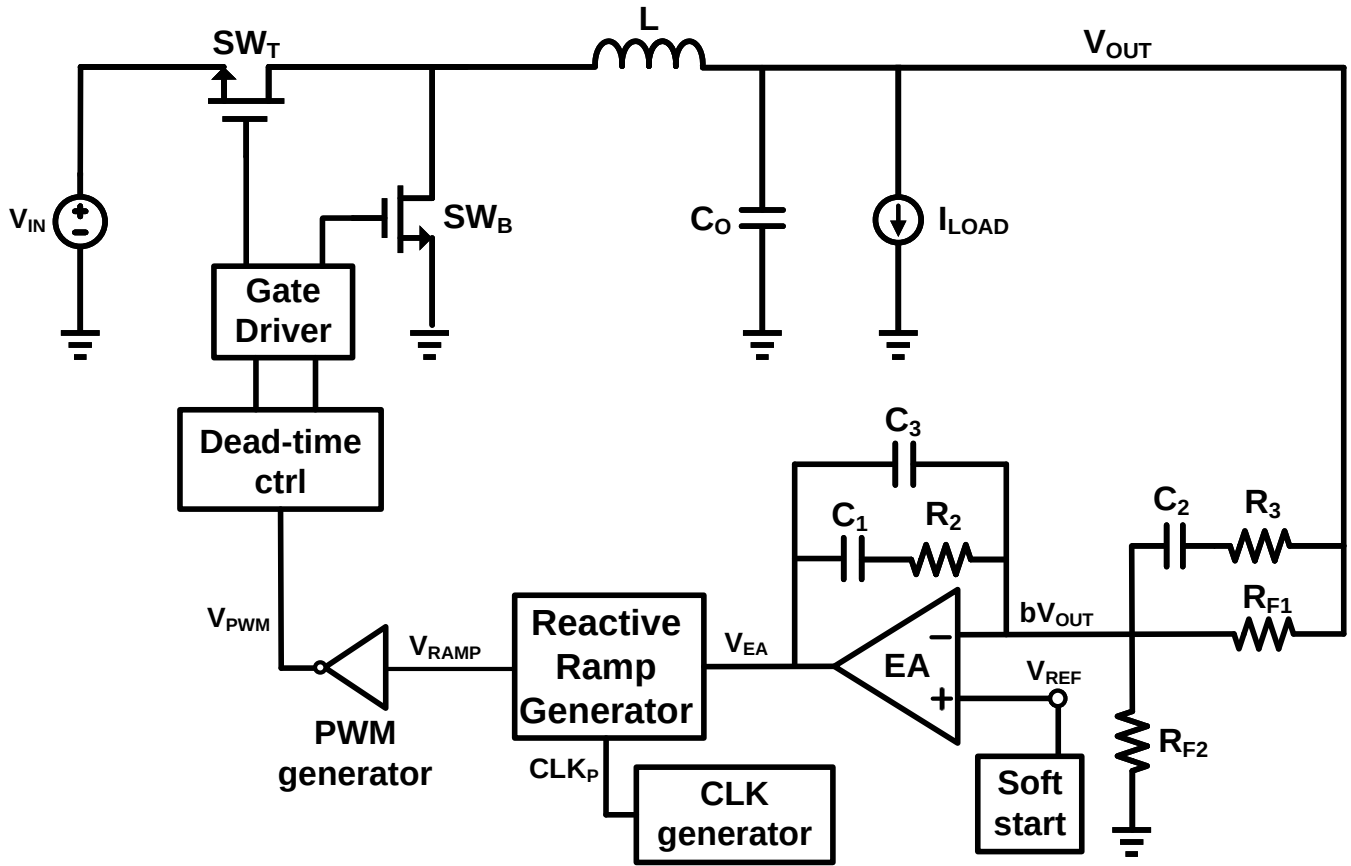


Figure 6. Comparator-less RRG-based buck converter block diagram.

3.1. Reactive Ramp Generator Circuit

To produce a ramp signal with a peak that dynamically adjusts according to the output voltage, we employ a reactive ramp generator, as shown in Figure 7a. In steady-state operation, the output of the error amplifier oscillates slightly with the switching operation while maintaining a specific DC level. When the load current, I_{LOAD} , suddenly increases, C_O discharges quickly, causing V_{OUT} to drop. The increased input difference at the error amplifier raises V_{EA} , prompting the RRG to generate a ramp signal with a lower V_M , which produces a larger duty cycle D for fast recovery of the output voltage. Conversely, when the load current demand decreases, V_{OUT} rises, decreasing V_{EA} . To bring the output voltage back down, a ramp signal with a higher V_M is generated, resulting in a smaller duty cycle D . The ramp amplitude V_M depends on the charge in C_R when CLK_P is low, with charging current I_{CHG} determined by the current mirror ratio k , transconductance g_{m1} of transistor M1, and gain A_v of the error amplifier, as given by Equation (2). The peak of V_M is a function of C_R , switching frequency f_{sw} , and I_{CHG} , as shown in Equation (3). Adjusting the gain of the RRG by tuning the current mirror ratio, transconductance, and error amplifier gain is essential to optimize the transient response without limiting the output range.

$$I_{CHG} = k \cdot g_{m1} \cdot A_v (V_{REF} - bV_{OUT}) \quad (2)$$

$$V_M = \frac{k \cdot g_{m1} \cdot A_v \cdot (bV_{OUT} - V_{REF})}{C_R \cdot f_{sw}} \quad (3)$$

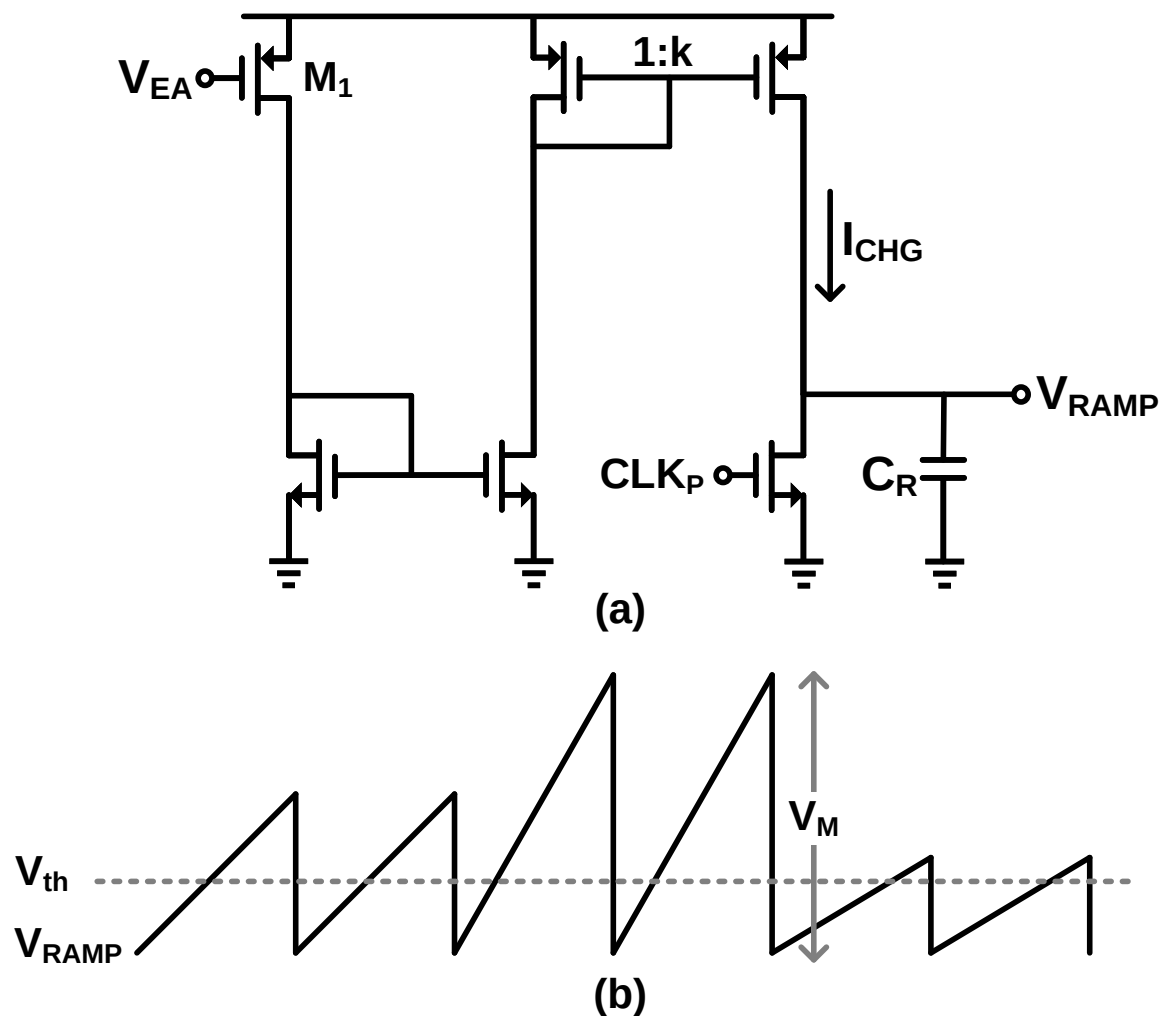


Figure 7. (a) Reactive ramp generator, **(b)** waveform of V_{RAMP} .

3.2. PWM Controller with Inverter

To mitigate the effects of comparator delay in high-frequency buck converters, the proposed design utilizes an inverter to generate the PWM signal that controls the power switch, driven by the ramp signal from the RRG. This approach prevents the SR latch violations previously discussed, allowing for minimal delay without the need to increase comparator tail current. Using an inverter instead provides a shorter delay with lower power consumption, improving efficiency.

Figure 8 shows the relationship between V_{th} and V_M . The duty cycle D , defined by the ratio of time t (when V_{RAMP} meets V_{th}) to the cycle period T , adjusts according to the difference between V_{REF} and bV_{OUT} , enabling the RRG to adjust V_M instantly during load transients, facilitating rapid output regulation.

$$D = \frac{t}{T} = \frac{V_{th}}{V_M} = \frac{C_R \cdot f_{SW} \cdot V_{th}}{k \cdot g_{m1} \cdot A_v \cdot (V_{REF} - bV_{OUT})} \quad (4)$$

In contrast to conventional voltage-mode buck converters, where the loop transfer function is defined by a fixed ramp V_M , the proposed structure dynamically adjusts V_M based on V_{EA} . As shown in Equation (5), derived from Equations (3) and (4), the difference

in the loop transfer function primarily affects the DC gain, allowing loop stability to be achieved using a standard type-3 compensation method.

$$\begin{aligned}
 T(s) &= A(s) \cdot b \cdot \frac{1}{D} \cdot \frac{V_o}{V_M} \cdot \frac{1 + \frac{s}{w_z}}{1 + \frac{1}{Q} \cdot \frac{s}{w_o} + \left(\frac{s}{w_o}\right)^2} \\
 &= A(s) \cdot b \cdot \frac{V_M}{V_{th}} \cdot \frac{V_o}{V_M} \cdot \frac{1 + \frac{s}{w_z}}{1 + \frac{1}{Q} \cdot \frac{s}{w_o} + \left(\frac{s}{w_o}\right)^2} \\
 &= A(s) \cdot b \cdot \frac{V_o}{V_{th}} \cdot \frac{1 + \frac{s}{w_z}}{1 + \frac{1}{Q} \cdot \frac{s}{w_o} + \left(\frac{s}{w_o}\right)^2}
 \end{aligned} \tag{5}$$

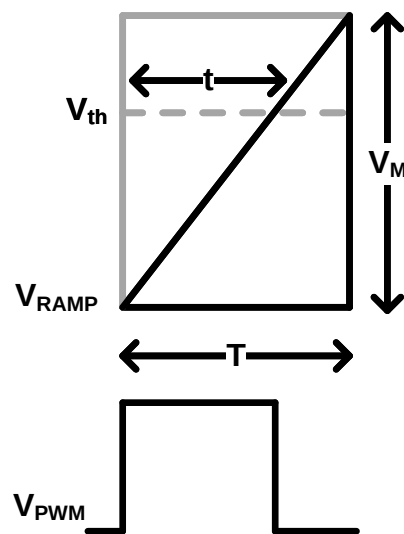


Figure 8. Duty cycle relationship between V_M and V_{th} .

3.3. Type-3 Compensator with Error Amplifier

In a voltage-mode buck converter, the transfer function of the power stage includes a pair of double poles determined by the inductor, L , and the output capacitor, C_o , as well as a zero introduced by the equivalent series resistance (ESR) of C_o . Without proper compensation, these characteristics lead to instability and degraded transient performance. To counteract this, a type-3 compensator is widely adopted, as it introduces two zeros to cancel the double poles and two additional poles to counteract the ESR zero and provide sufficient roll-off at higher frequencies, ensuring stability and robust transient response.

The error amplifier, shown in Figure 9, plays a central role in the type-3 compensator design by providing high open-loop gain and wide bandwidth. The amplifier employs a folded cascode topology. This helps maintain a stable phase margin and ensures rapid response to load transients. The amplifier's wide bandwidth allows for quick adjustment to load changes, contributing to both efficient operation and robust performance under varying load conditions. The biasing voltages (V_{B1} , V_{B2} , V_{B3} , V_{B4}) ensure stable operation over a wide range of input conditions, while cascode transistors improve the output impedance and enhance gain.

The output of the error amplifier (V_{EA}) is designed to interface the RRG, with its range constrained to ensure that the M1 transistor in the RRG satisfies the saturation condition. The cascode compensation nodes (V_{PCAS} , V_{NCAS}) further stabilize the operation by improving frequency response and reducing susceptibility to noise. These nodes play a critical role in ensuring proper biasing and reducing the effect of parasitics, especially at high frequencies. Additionally, the wide bandwidth of the error amplifier allows it to

quickly respond to rapid changes in load conditions, minimizing output voltage deviations during transient events. This precise control ensures both stable loop operation and enhanced efficiency in high-performance buck converter applications.

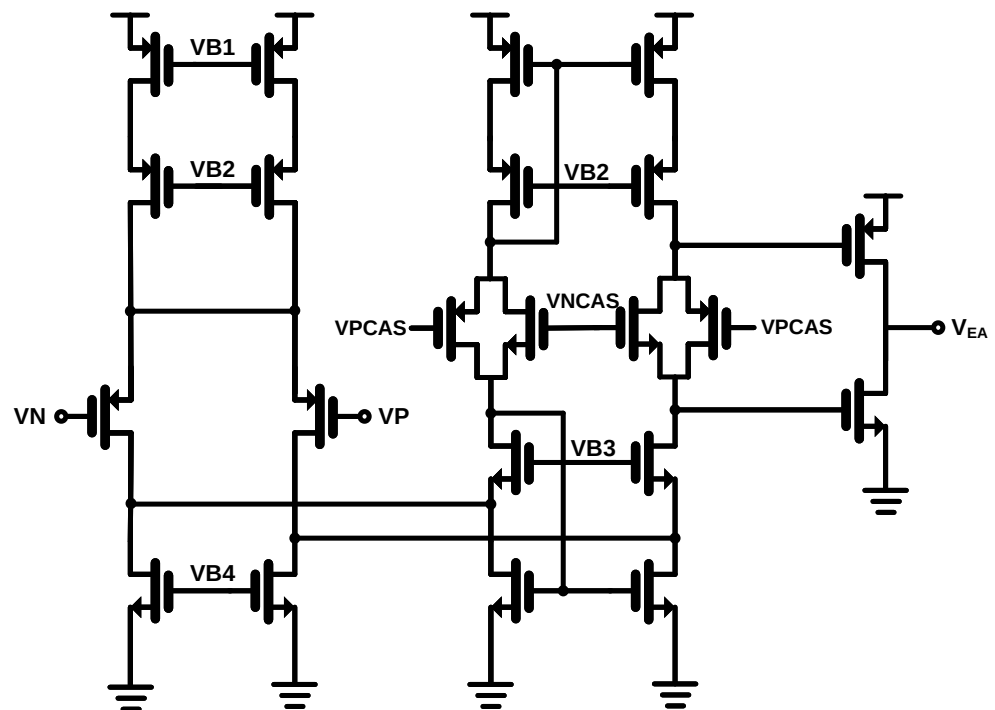


Figure 9. Schematic of folded cascode error amplifier.

To further optimize the drive capability of the error amplifier, a class-AB buffer stage is integrated at its output. The class-AB buffer provides high output current drive while maintaining low quiescent current, effectively enhancing the error amplifier's ability to drive capacitive loads, such as the input of RRG. This ensures V_{EA} maintains its integrity across varying load conditions, contributing to both transient performance and overall system stability. The folded cascode topology, combined with the class-AB buffer and external compensation components, offers the flexibility and robustness for demanding high-frequency buck converter designs.

3.4. Deadtime Controller

Figure 10 illustrates the architecture of a dead time controller, a critical component in buck converters designed to prevent shoot-through current. Shoot-through current occurs when the high-side switch (SW_T) and low-side switch (SW_B) are simultaneously active, creating a direct short between the input supply and ground. To solve this problem, the dead-time controller ensures that SW_T and SW_B do not conduct at the same time by introducing a delay between their switching events. The circuit achieves this functionality by processing the PWM control signal (V_{PWM}) through a combination of logic gates, inverters, and delay blocks.

This timing relationship is illustrated in Figure 11, which shows the waveforms of V_{PWM} , SW_T , and SW_B . The dead time, highlighted in red, represents the interval when neither switch conducts. By implementing this delay, the controller prevents power losses due to body diode conduction and eliminates the risk of destructive shoot-through current. Additionally, the dead-time optimization enhances overall system efficiency and stability by ensuring seamless transition between switching events.

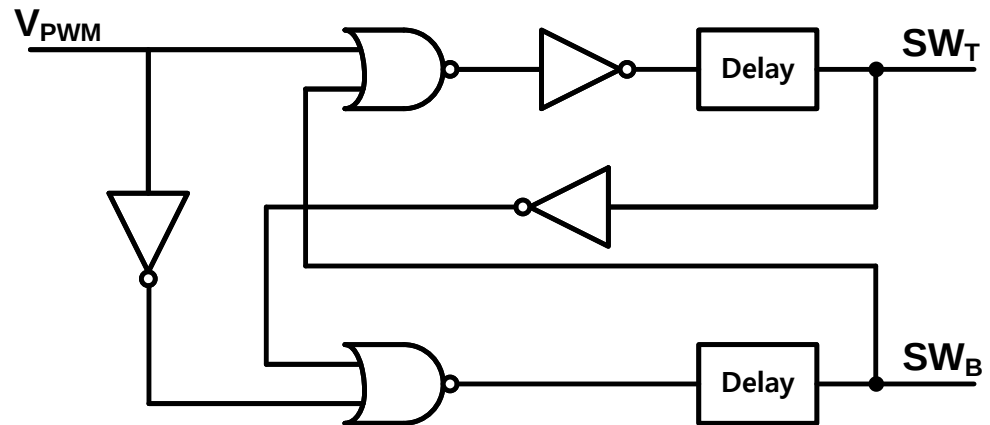


Figure 10. Deadtime controller circuit.

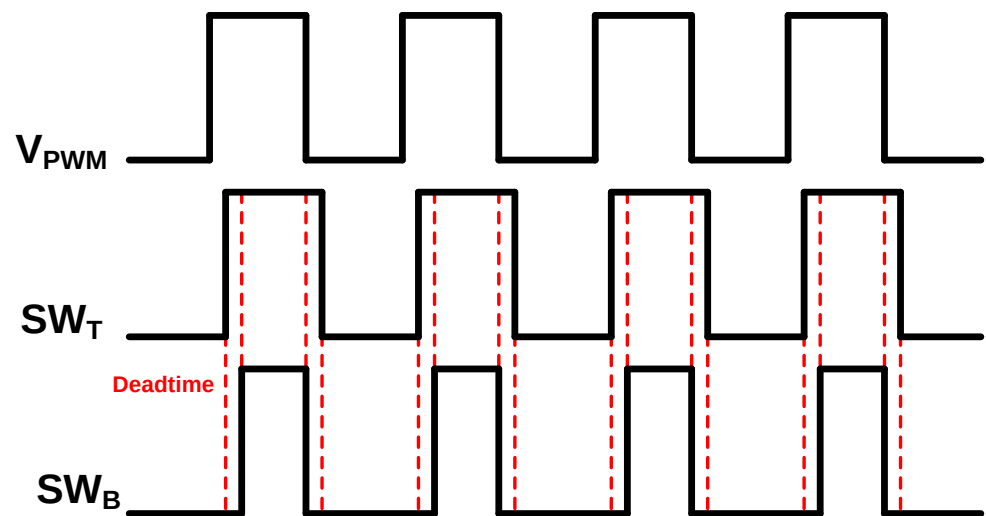


Figure 11. Timing diagram of V_{PWM} , SW_T , and SW_B .

3.5. Soft Start Circuit

A soft start circuit is an essential component in buck converters to ensure a controlled and smooth startup by preventing excessive inrush current and output voltage overshoot [20]. Figure 12a illustrates the proposed soft start mechanism, which employs a slope generator to produce a gradually increasing reference signal (V_{RAMPSS}). During the startup phase, this ramp signal is compared with the fixed reference voltage (V_{REF}) in a comparator. The output of the comparator enables the appropriate control signal (V_{REFSS}), which regulates the duty cycle of the converter. By gradually increasing V_{REFSS} , the output voltage rises linearly, ensuring stable operation and protecting both the circuit components and the load.

Figure 12b shows the timing relationship between V_{RAMPSS} , V_{REF} , and V_{REFSS} . Initially, V_{RAMPSS} starts from zero and increases with a defined slope until it reaches V_{REF} . This controlled ramping prevents sudden voltage surges that could otherwise cause high inrush currents and potential damage to the switching elements or the output capacitor. Once V_{RAMPSS} surpasses V_{REF} , the system transitions to normal operation, maintaining V_{REF} for steady-state regulation.

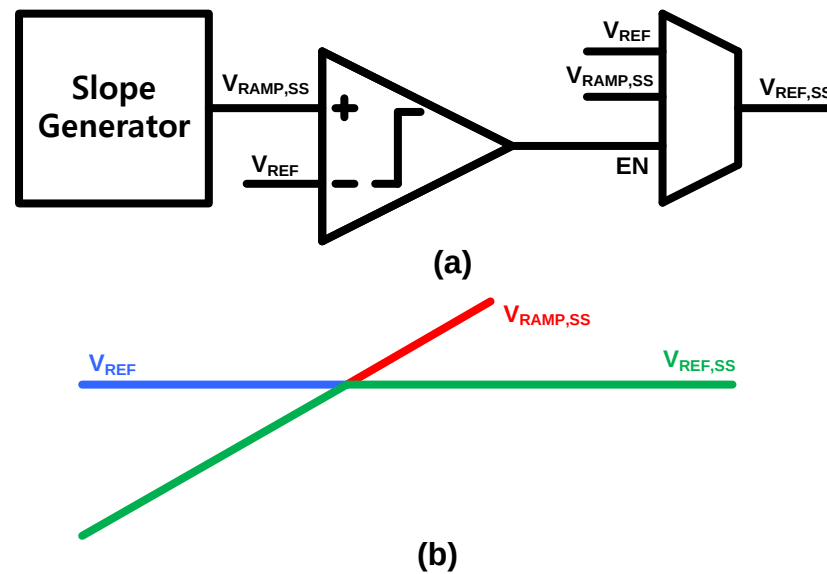


Figure 12. (a) Soft start circuit schematic; (b) soft start waveform.

4. Performance Results

The proposed RRG-based voltage-mode buck converter is fabricated using a standard 0.18 μm CMOS process. Figure 13 shows the chip micrograph, with a total area of 1.5 mm^2 (1.5 $\text{mm} \times 1 \text{ mm}$), including bonding pads.

This buck converter employs a 470 nH inductor and a 1 μF output capacitor, operating with an input voltage of 3.3 V. The regulated output voltage range is 0.8 V to 3.2 V, supporting a maximum load current of 1.5 A. The output voltage range spans from 0.65 V to 3.0 V, with duty cycle D covering a range of 0.27 to 0.98, offering a wide duty range of 0.71. At an output voltage of 1.8 V, the measured output ripple is 2 mV, demonstrating the design's effectiveness in minimizing noise. Figure 14 presents the load transient simulation when the load current steps from 200 mA to 1 A and back from 1 A to 200 mA, with V_{IN} set at 3.3 V and V_{OUT} at 1.8 V. The up-transient response time is 0.802 μs , while the down-transient response time is 1.27 μs , with an undershoot of 114 mV and an overshoot of 154 mV.

Figure 15 illustrates the simulated waveform of V_{RAMP} for different output voltages. The peak values of V_{RAMP} are 1.73 V, 1.28 V, and 0.88 V for output voltages of 1.2 V, 2.0 V, and 2.8 V, respectively.

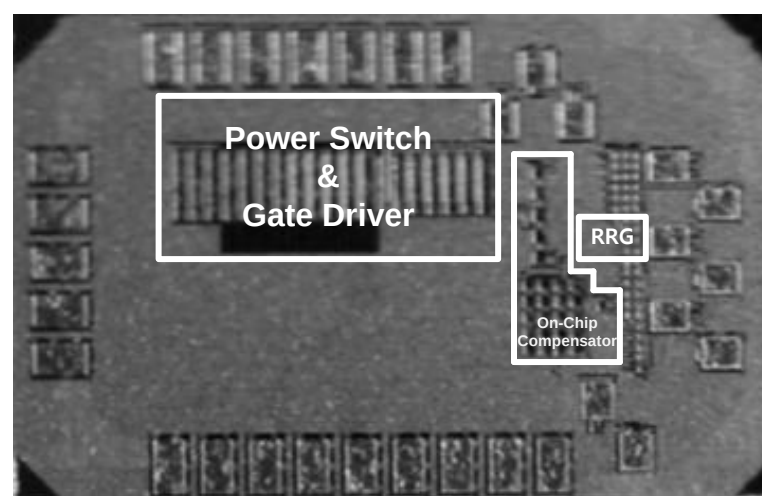


Figure 13. Chip microphotograph.

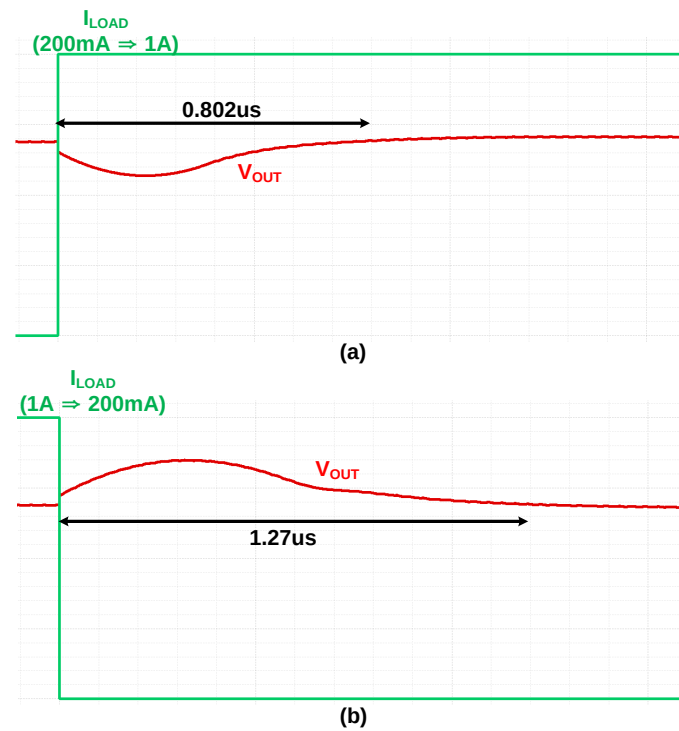


Figure 14. Load transient response (a) 200 mA $\rightarrow$ 1A, (b) 1A $\rightarrow$ 200 mA load current changes.

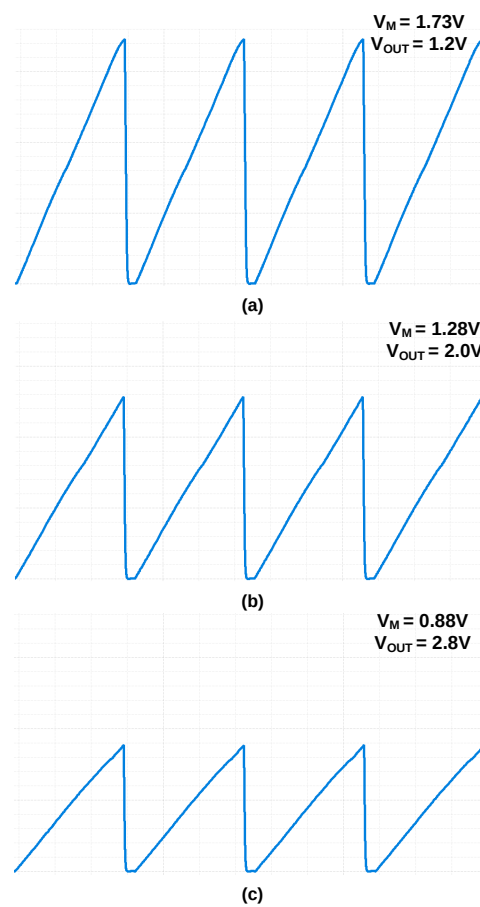


Figure 15. Reactive ramp generator waveform corresponding to output voltage (a) $V_{OUT} = 1.2$ V, (b) $V_{OUT} = 2.0$ V, (c) $V_{OUT} = 2.8$ V.

Figure 16 illustrates the behavior of V_{RAMP} during load transient conditions. In Figure 16a, when the load current increases from 200 mA to 1 A, the output voltage momentarily drops due to the discharge of C_O . To restore the output voltage to the desired level, a V_{RAMP} signal is generated to produce a larger duty cycle. Specifically, a V_{RAMP} signal lower than V_{th} is used to regulate the output voltage effectively. Conversely, Figure 16b depicts the scenario when the load current decreases from 1 A to 200 mA. In this case, the output voltage rises due to the reduced current demand. To lower the output voltage, a V_{RAMP} signal is generated to produce a smaller duty cycle. This dynamic adjustment of V_{RAMP} ensures stable regulation of the output voltage during both load increase and decrease events.

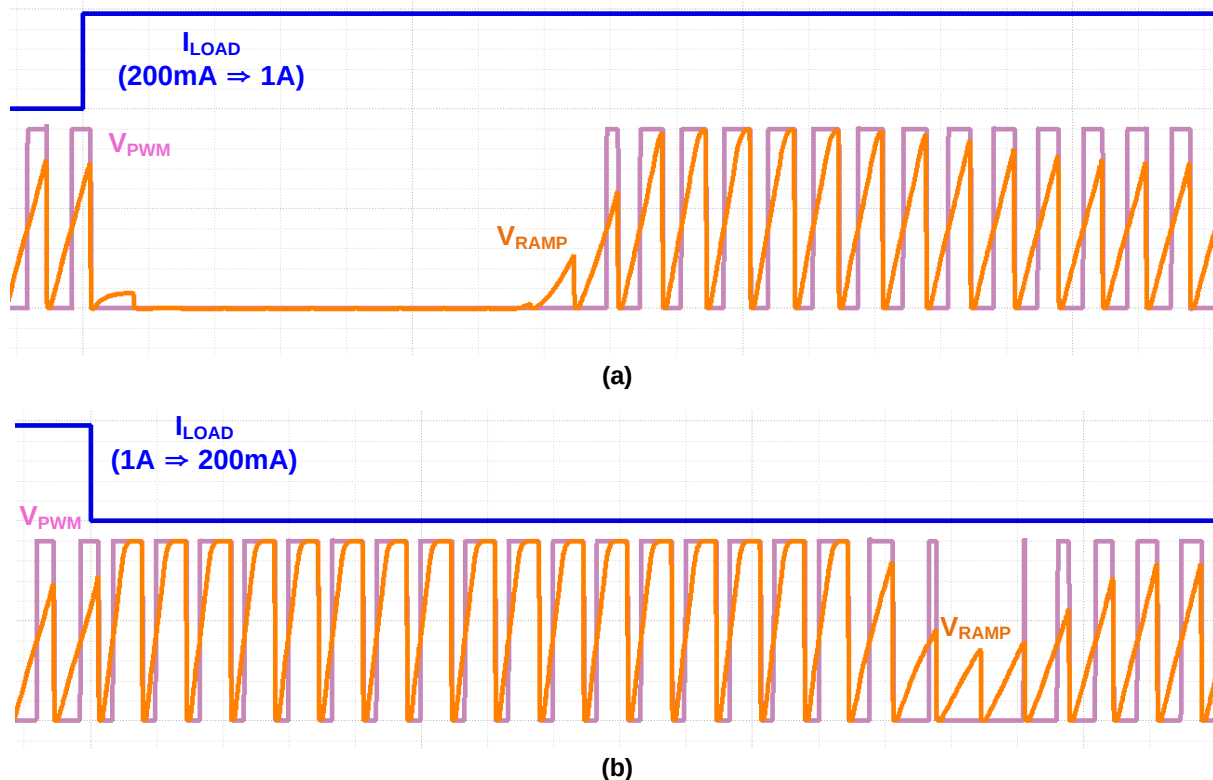


Figure 16. Simulated waveform of V_{OUT} under load transient situation (a) 200 mA $\rightarrow$ 1 A, (b) 1 A $\rightarrow$ 200 mA.

Figure 17 shows the simulated efficiency across various load currents and output voltages at a 30 MHz switching frequency, demonstrating a peak efficiency of 92.78% under conditions of 2.4 V output and 600 mA load current.

In the inverter-based PWM controller, D is set by the ratio of the error amplifier output to V_{th} . The circuit's performance remains stable against variations in inverter threshold due to PVT changes, as negative feedback from the error amplifier governs the overall circuit behavior. Figure 18 shows simulation results, demonstrating the linear relationship between V_{OUT} and D across ss, tt, and ff corners.

The aforementioned performance metrics of the proposed high-frequency buck converter circuit are summarized in Table 1. By incorporating the RRG, which adapts to changes in V_{OUT} , the proposed design achieves a faster transient response than conventional high-frequency buck converters, even when subjected to a load step twice as large. The removal of a comparator from the feedback path eliminates potential delays associated with comparator operation, further ensuring that the system responds rapidly to changes in load conditions.

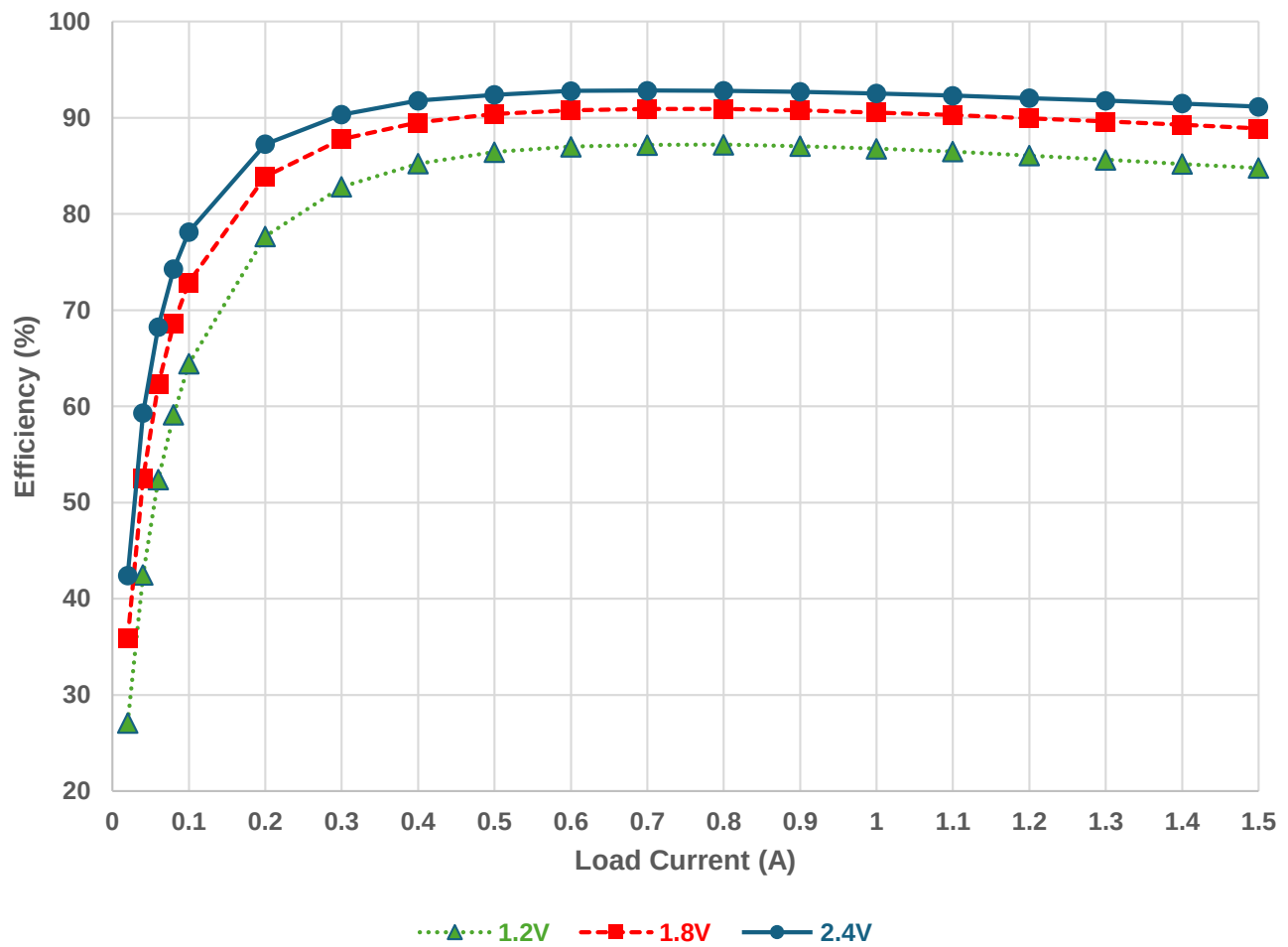


Figure 17. Efficiency of the proposed converter.

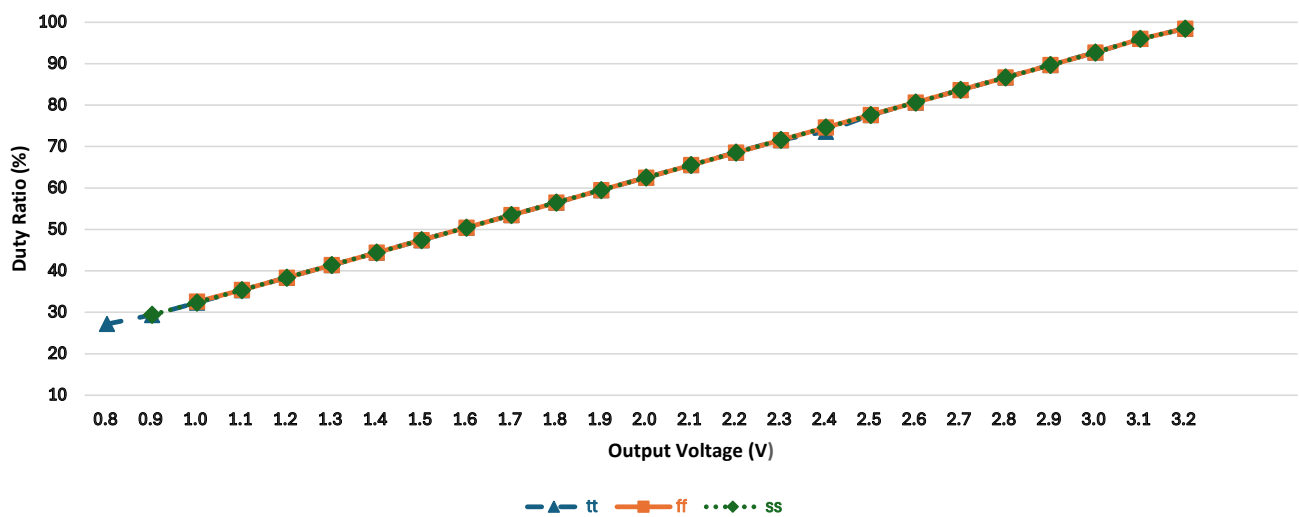


Figure 18. Simulation results across different corners about relationship between D and V_{OUT} .

Table 1. Performance summary and comparison.

	This Work	2024 TCAS II [12]	2018 TCAS II [11]	2015 JSSC [21]	2014 JSSC [9]
Technology	180 nm	180 nm	180 nm	65 nm	130 nm
Power Supply	3.3 V	3.3 V	3.3 V	1.8 V	3.3 V
L	470 nH	220 nH	90 nH	90 nH x4	330 nH
C _O	1 µF	1 µF	2.2 µF	0.47 µF	1 µF
Frequency	30 MHz	10~30 MHz	30 MHz	30~70 MHz	10/30 MHz
Output Voltage	0.65~3 V	0.2~3 V	0.4~2.8 V	0.6~1.5 V	0.45~2.4 V
Duty Range	0.714	0.85	0.744	X	0.59
Load Transient Step	800 mA	300 mA	400 mA	400 mA	340 mA
Settling Time	0.802 µs/1.27 µs	4 µs	3 µs	0.6 µs	5 µs
* Overshoot	154 mV (6.55%)	42.5 mV (1.52%)	95 mV (3.96%)	90 mV (10%)	30 mV (1.54%)
* Undershoot	114 mV (4.85%)	50 mV (1.79%)	110 mV (4.58%)	80 mV (8.89%)	50 mV (2.56%)
Peak Efficiency	92.78%	90.6%	90.2%	87%	86.6%

* Overshoot/Undershoot (%) = $\frac{\text{Overshoot or Undershoot (mV)}}{V_{\max} - V_{\min}} \times 100$ where $V_{\max}$ and $V_{\min}$ are the maximum and minimum output voltages, respectively.

5. Conclusions

This paper presents a high-frequency buck converter based on a Reactive Ramp Generator (RRG), specifically designed to achieve fast transient response by addressing the limitations of comparator delay—a critical bottleneck in high-frequency converters. The proposed design utilizes a comparator-less reactive ramp generator and an inverter-based PWM controller, eliminating the delays associated with conventional comparators. The RRG dynamically adjusts V_{RAMP} based on output voltage variations, and, together with a short feedback loop, enables a rapid and stable load transient response.

Performance results demonstrate reliable operation across a range of voltage and load current conditions. In response to load step-up and step-down events, the converter achieves settling times of 0.802 µs and 1.27 µs, respectively, with a peak efficiency of 92.78% at 2.4 V output. These simulated results confirm that the proposed RRG-based buck converter delivers faster transient response and higher efficiency compared to conventional high-frequency buck converters, making it a promising solution for modern high-speed power management applications.

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Abbreviations

The following abbreviations are used in this manuscript:

C_o	Output Capacitor
DVFS	Dynamic Voltage and Frequency Scaling
ESR	Equivalent Series Resistance
L	Inductor
PVT	Process, Voltage, and Temperature
PWM	Pulse Width Modulation
RRG	Reactive Ramp Generator
SW_T	High-side Switch
SW_B	Low-side Switch
V_{EA}	Error Amplifier Output Voltage
V_M	Maximum Value of the Ramp Signal
V_{PWM}	PWM Signal Voltage
V_{REF}	Reference Voltage for Output Voltage
V_{RAMP}	Ramp Signal Voltage

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